DS1 Test Patterns

Introduction

DS1 test patterns are predetermined, repeating one and zero bit sequences that are translated into pulses according to the line coding rules for AMI and B8ZS. A test pattern is transmitted from one end and should be received error-free at the other end. Test patterns also can be used when a circuit is looped back, in which case the transmitted pattern is received by the same test set.

Test patterns are designed to

- Test for proper line code optioning (AMI or B8ZS)
- Stress DS1 interfaces at their maximum and minimum pulse densities to reveal malfunctioning equipment
- Uncover random performance anomalies due to environmental conditions, synchronization problems or crosstalk

A DS1 interface usually is first tested for proper line code optioning (typically for a few seconds) and then stress tested (for at least 15 minutes) for performance. ANSI T1.510 specifies test lengths and requirements for performance measurements [1]. The actual test patterns to be used will depend on the test situation.

Various test patterns are briefly described below. More complete descriptions can be found in [2] and [3]. The test patterns are categorized as *Common Test Patterns*, *Specialty Test Patterns*, *Channel Test Patterns* and *DDS Test Patterns*. The *Common Test Patterns* are used most often. No single test pattern will completely test a DS1 interface, so several patterns may be required.

Not all test sets have all test patterns and some test sets have extra-cost test pattern options. Also, the test patterns in some test equipment may not be compatible with test patterns having the same name in other equipment. Therefore, if two different test sets are used in end-to-end tests, particularly if different manufacturers make them, they should be connected back-to-back and tested for pattern compatibility.

Common Test Patterns

The *Common Test Patterns* described below are used to test DS1 interfaces upon initial installation and after repair.

3-in-24 – A repeating 24-bit sequence that contains three ones, fifteen consecutive zeros and 12.5% average ones density. This pattern is used primarily to test clock recovery and may be used framed or unframed. This pattern will invoke the B8ZS line code if transmitted through interfaces optioned for B8ZS.

1:7 (also written as 1-in-8) – An 8-bit pattern that contains a single one and is used primarily to test clock recovery and may be used framed or unframed. When transmitted unframed the pattern has a maximum of seven zeros, and the pattern will not force the B8ZS line code. When transmitted framed, framing bits can force the maximum number of consecutive zeros to eight, and the pattern will invoke the B8ZS code in interfaces optioned for B8ZS.

2-in-8 – An 8-bit pattern in which the second and seventh bit positions contain a one and all other positions contain zeros. This pattern is specified in industry job aids (see [2]) to verify proper AMI and B8ZS optioning, but otherwise is little used. It is not available in all test sets.

QRSS (also written QRS or QRW) – The QRSS (quasi-random signal source) is the most common pattern for DS1 interface testing. It is a pseudo-random bit sequence based on a 20-bit shift register. It repeats every 1,048,575 bits and contains no more than fourteen consecutive zeros with both high and low density sequences. This pattern stresses clock recovery circuits, automatic line build-out (ALBO) and equalizer circuits, and it also simulates voice traffic. The QRSS pattern can be used framed or unframed and will invoke a B8ZS code in interfaces optioned for B8ZS.

ALL ONES – An unframed pattern that has ones in all payload bit and frame bit positions. It causes transmitter circuitry to consume the maximum possible power. In a T1-Carrier span with line- powered repeaters, this pattern will verify that the dc power is regulated correctly. An All-Ones pattern is the same as an Alarm Indication Signal (AIS) or "Blue Alarm," which is sent forward by an interface that has lost its input signal. It will never invoke the B8ZS line code. This pattern only should be used in isolated segments of a transmission system and not in transmission chains; otherwise, it may produce unpredictable results.

ALL ZEROS – A framed pattern having all payload (non-framing) bit positions set to zero. The pattern is used to verify that all interfaces in a transmission chain are optioned for B8ZS. If any interface in the chain is incorrectly optioned for AMI, it will fail immediately because no pulses are available for clock recovery.

T1-DALY and 55 OCTET – The 55 OCTET pattern also is called T1-6. These two patterns each contain 55-octets (an octet is an 8-bit word) in a sequence that changes rapidly between low and high ones density. They both are used to stress the ALBO and equalizer circuitry but they also stress clock recovery circuits. The 55-OCTET pattern contains bit sequences with fifteen consecutive zeros and violates the 12.5% ones-density requirements on AMI interfaces. The T1-DALY pattern is very slight modification of the 55-OCTET pattern (it differs by only one bit) and meets the 12.5% ones-density requirement. Both patterns will invoke a B8ZS line code in circuits optioned for B8ZS.

Specialty Test Patterns

Sequences of predefined test patterns are used to quickly test a DS1 interface or provide bit sequences for bridged tap detection and pulse-shape measurements.

1-in-16 (also written as 1:15) – A 16-bit pattern with a single one followed by 15 zeros. This test pattern is seldom used except to detect mistuning in older T1-Carrier line repeaters. It is not available in all test sets.

MULTIPLE PATTERN (also written as MULITPAT[1]) – A pattern consisting of five patterns (ALL ONES, 1:7, 2-in-8, 3-in-24 and QRSS) where each pattern is transmitted for 180 seconds

[1] MULTIPAT is a registered trademark of Acterna (formerly Telecommunications Techniques Corp.)

and monitored for 175 seconds. The results are reported for each individual pattern and on the entire sequence.

Q-TEST or QUICK TEST – A sequence of the patterns described in the *Common Test Patterns* section. Each pattern is executed for five seconds. ALL ZEROS is only executed when the B8ZS option is set. The sequence is used to quickly determine the probability of a circuit passing a full conformance test. The Quick Test may not be available on all test sets.

T1-2 (Also called TRIP) – A test pattern consisting of 96 octets (768 bits) in which the first 48 octets contain all ones (high density) followed by four octets of alternating one-zero sequence, followed by 20 octets that contain repeating sequences of 15 zeros in a row (low density), followed by four octets of alternating one-zero sequence, followed by 20 octets that contain repeating sequences of 15 zeros in a row (low density). This pattern exercises transmitter output and receiver clock recovery circuits. It will not cause a low-density (excess zeros) alarm in circuits optioned for AMI but it will invoke a B8ZS line code in circuits optioned for B8ZS.

T1-3 – This test pattern is similar to T1-2 except it only contains 54 octets the majority of which are repeating sequences of 15 zeros in a row. This pattern exercises receiver clock recovery circuits. It will not cause a low-density (excess zeros) alarm in circuits optioned for AMI but it will invoke a B8ZS line code in circuits optioned for B8ZS

T1-4 – The T1-4 pattern is 120 octets (960 bits) long of which the first 72 octets are all ones followed by four octets with alternating one-zero sequence, followed by 20 octets in which all bits are zero except the fourth bit, followed by four octets with alternating one-zero sequence, followed by 20 octets in which all bits are zero except the fourth bit. This pattern exercises transmitter output circuits. It will not invoke a B8ZS line code in circuits optioned for B8ZS nor will it cause a low-density alarm in circuits optioned for AMI.

T1-5 – This pattern is 53 octets long and it provides rapid transition from high density to low density bit sequences. This pattern exercises clock recovery circuits. It will invoke a B8ZS code in circuits optioned for B8ZS but will not cause a low-density alarm in circuits optioned for AMI.

BRIDGED TAP – Used to detect the presence of a bridged tap on a circuit that has been converted from an analog application to T1-Carrier. The sequences effectively generate a series of analog tones that resonate the bridged tap. At resonance, the bridged tap usually but not always will cause bit errors or bipolar violations. The sequence consists of 21 patterns starting with ALL ONES and ending with QRSS. Each pattern is transmitted for 30 seconds and monitored for 23 seconds. The results are reported for each individual pattern and on the entire sequence. Interface and test set B8ZS options must be turned OFF for this sequence to be effective in detecting bipolar violations.

PULSE SHAPE CONFORMANCE – Test patterns that minimize the effects of inter-symbol (adjacent signal) interference that could disturb the DS1 pulse shape measurement. It should be used whenever pulse shapes are measured against a pulse mask. This pattern consists of a repeating sequence of 8 bits with bit position 5 set to one and all other bit positions set to zero. The isolated one produces a single pulse surrounded by seven zeros in the repeating sequence. Not all test sets have this pattern; however, any test set that has T1-3, T1-4, T1-5, T1-6 (55 OCTET), T1-DALY or MIN/MAX will provide sufficiently isolated pulses.

Channel Test Patterns

Channel test patterns normally are not used to test DS1 interfaces because they violate ones density or consecutive zeros requirements. However, they may be used to simulate user traffic on Fractional T1 circuits and on individual DS-0 channels when the test set is in a Drop/Insert mode or for testing E1 (2048 kb/s) network gateways.

2047 – A pseudorandom sequence based on an 11-bit shift register.

2E15-1 (also written 2^{15}-1) – A pseudorandom sequence based on a 15-bit shift register.

2E20-1 (also written 2^{20}-1) – A pseudorandom sequence based on a 20-bit shift register.

2E23-1 (also written 2^{23}-1) – A pseudorandom sequence based on a 23-bit shift register.

FOX – A pattern consisting of 8-bit ASCII characters formed into a text message with all alpha-numerics (letters and digits) - "THE QUICK BROWN FOX JUMPS OVER THE LAZY DOG 1234567890". The FOX pattern was used with teleype circuits and is seldom used with modern equipment.

DDS Test Patterns

DDS patterns are primarily used to test individual channels that are configured as DS-0A or DS-0B for Dedicated Digital Service (DDS) circuits operating at 64 kb/s or less. These patterns are used with the test set in a Drop/Insert mode.

DDS-1 – A 200-octet pattern consisting of 100 octets of all ones followed by 100 octets of all zeros. It is used to stress the signal and clock recovery capability of DDS circuits.

DDS-2 – A 200-octet pattern consisting of 100 octets of 7Eh (0111 1110) followed by 100 octets of all zeros. This pattern simulates bit oriented protocol flags for DDS testing.

DDS-3 – A 16-octet pattern consisting of a continuous stream of medium ones density octets. Each octet is 4Ch or 0100 1100. It is used to simulate a typical DDS signal.

DDS-4 – A 16-octet pattern consisting of low-density octets. Each octet is 40h or 01000000. It is used to stress DDS clock recovery.

DDS-5 – A 2000-octet pattern consisting of 800 0ctets of DDS-1, 800 octets of DDS-2, 200 octets of DDS-3, and 200 octets of DDS-4. It is used as a quick test of DDS circuit operation.

DDS-6 – An 8-octet pattern consisting of seven octets of FEh (1111 1110) followed by one octet of FFh (1111 1111). It is used to simulate the transition from IDLE mode to DATA mode in a DDS signal.

Appendix – AMI and B8ZS Line Codes

When the AMI line code is used on a DS1 interface, the individual channels are limited to 56 kb/s because one of the payload bits in each channel (timeslot) is set to a logic 1 to ensure clock recovery at the receiver. The B8ZS line code overcomes this limitation and allows Clear Channel Capability (CCC) in which all channels can be operated at the full 64 kb/s rate. B8ZS ensures that enough pulses are available for clock recovery at the receiver and is used whenever possible (older equipment may not support B8ZS).

B8ZS uses the same basic line coding rules as AMI except that B8ZS substitutes two bipolar violations (which are not allowed with AMI) and two normal pulses whenever the transmitted bit stream contains eight zeros in a row. Since the B8ZS line code only is invoked when the bit stream contains eight zeros in a row, the interface will appear to be optioned for AMI at all other times.

To ensure clock recovery on DS1 interfaces, ANSI Standard T1.102 requires an average pulse density of 12.5% (an average of one pulse in eight bit positions) with no more than 15 consecutive zeros (no pulses). The primary reason for this ones density requirement is clock recovery but other factors, such as automatic-line-build-out (ALBO), equalization, and power consumption, also require an adequate ones density.

References:

[1] ANSI T1.510, Network Performance Parameters for Dedicated Digital Services for Rates Up to and Including DS3 – Specifications, 1999.
[2] Technical Report No. 25, Test Patterns for DS1 Circuits, ATIS, Nov. 1993.
[3] T-BERD® 224 User's Guide, Acterna (formerly Telecommunications Test Corp.).

Document Information

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