DS-1 Relative Timing Measurements

I - Introduction

a. General:

This application note describes relative timing measurements using DS-1 test sets. Test sets covered are:

- TTC T-BERD 224 – Section II
- Sunset T10 – Section III
- Hewlett Packard 37702A – Section IV
- TTC T-BERD 2209 – Section V

All timing problems are manifested as errors, but not all errors are caused by timing problems. It sometimes is difficult to distinguish between errors caused by timing and other problems. However, all test sets are able to separately count logic errors, Bipolar Violations (BPV), framing bit errors, and frame slips. Frame slips always indicate a timing problem, while the other error types may be caused by interface or transmission problems unrelated to timing. An excessive error rate can cause loss of frame synchronization and Change of Frame Alignment (COFA) but usually will not affect timing slips count. If the error rate on an interface is so high that frame synchronization is impossible, it is likely the interface is faulty and it should be repaired before timing tests are made.

The following general discussion does not cover synchronization in detail. Additional information can be found in references [1] and [2] (listed at the end of this section).

b. Relative Timing Tests:

Most DS-1 test sets have provisions for measuring the relative timing between two interfaces. Measurements usually are based on a known good interface (reference DS-1 interface with timing traceable to a known good source, usually Stratum 1). See Figure I-1.

The test set compares the test signal with the reference and counts the number of times the clock edge of the received signal moves past the edge of the reference signal, as shown in Fig. I-2.

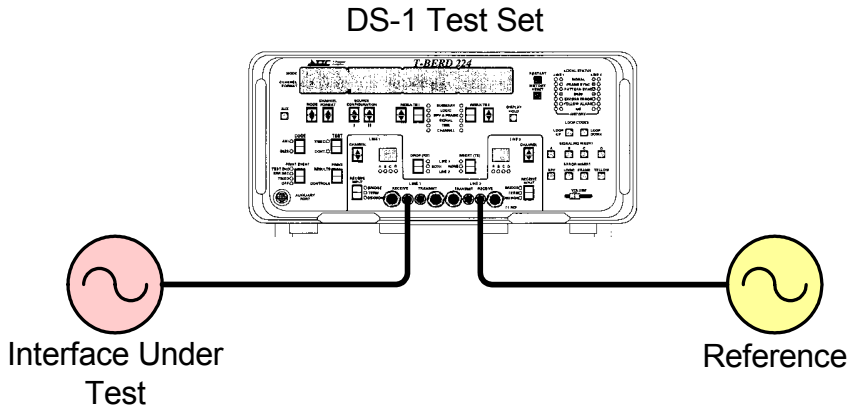
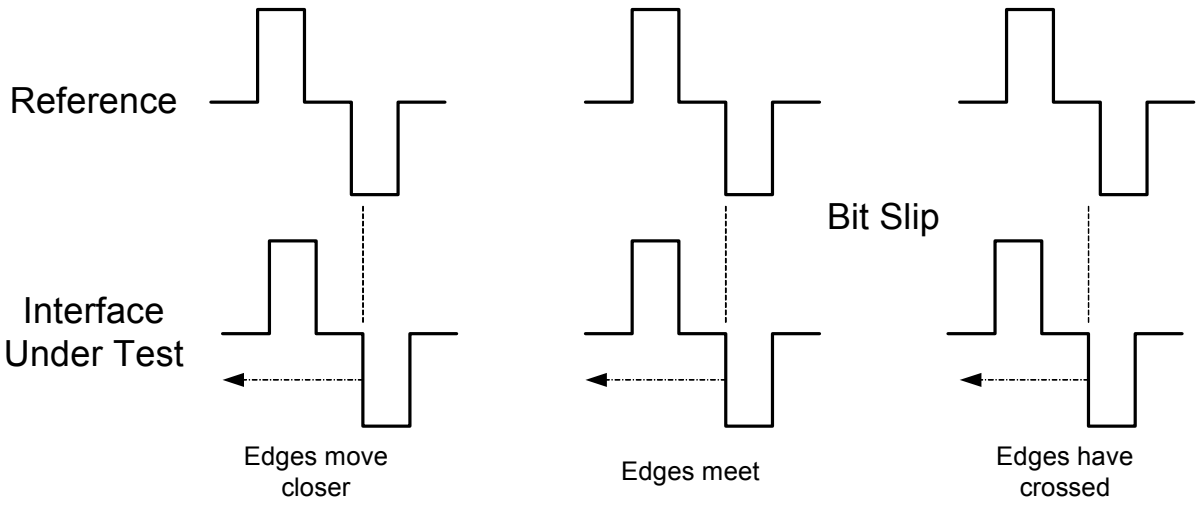


Figure I-1 – Relative Timing Tests

Figure I-2 – Bit-Slip



The test set usually displays a bar graph with moving cursor that shows the relative frequency difference between the reference and interface under test. If the cursor does not move, then the two interfaces operate at exactly the same rate and there is no wander. A moving display indicates a frequency difference. The faster the display moves, the larger the frequency difference between the two interfaces.

c. Timing Slips:

A bit- or clock-slip is the loss or gain of one bit period in a DS-1 interface relative to another interface due to a frequency or phase difference between the two interfaces. A single bit-slip or a few bit slips have no impact on a system because all DS-1 interfaces have buffers to absorb transient frequency differences. However, if the frequency difference (or offset) is sustained, the buffer eventually will overflow or underflow, leading to the loss or repetition of a number of bits equal to the buffer size. Most interfaces will absorb at least one full frame (192 payload bits plus one framing bit) but some equipment interfaces have 32 or 64 bit buffers.

A frame slip is the deletion or repetition of a full data frame (192 payload bits). A controlled frame slip means that frame boundaries are not lost and only payload bits are lost; that is, the framing bit is retained and the frame buffer is emptied of or filled with payload data as required. An uncontrolled slip means frame boundaries as well as payload are lost; that is the framing bit is lost and reacquisition of the frame is required.

Slips can occur when a network element, such as a switching system or digital cross-connect system, is connected to two or more DS-1 interfaces that are timed by different timing sources than the network element's timing source. If the timing sources are perfectly synchronized and there is no jitter or wander, then there will be no timing slips. If there are frequency or phase differences, timing slips will occur.

DS-1 Relative Timing Measurements

Slips are inevitable in digital networks but proper system design will minimize them. In a properly synchronized system, timing for all network elements is traceable to a Stratum 1 clock (but not necessarily the same Stratum 1 clock). If two DS-1 interfaces each are traceable to a different Stratum 1 clock, there will be no more than one frame slip in 72 days under worst-case conditions. If the timing source for one of the interfaces is not traceable to a Stratum 1 clock, frame slips will occur at a greater rate. For example, if one interface is traceable to a Stratum 1 clock and the other is traceable to a Stratum 3 clock (such as an end office switching system in free-run mode), there can be as many as 255 frame slips per day. See [1] or [2] for detailed calculations for other Stratum levels.

If the DS-1 interfaces operate over satellite, the timing quality will be reduced by satellite orbit wander. If the DS-1 interfaces operate over microwave radio relay systems, the timing quality will be reduced by propagation conditions and associated jitter and wander.

d. ***References:***

[1] Synchronization Model for Small Central Offices, Whitham D. Reeve, 2001.
[2] Telecommunications Synchronization Overview, Whitham D. Reeve, 2002.

Above documents are available from Reeve Engineers (www.reeve.com)

e. ***Revision History:***

Iss. 1 (July 17, 2002 original issue)
Iss. 2 (March 5, 2003 editorial corrections)
Iss. 3 (March 28, 2003 added TTC 2209)

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II - TTC T-BERD 224

a. General:

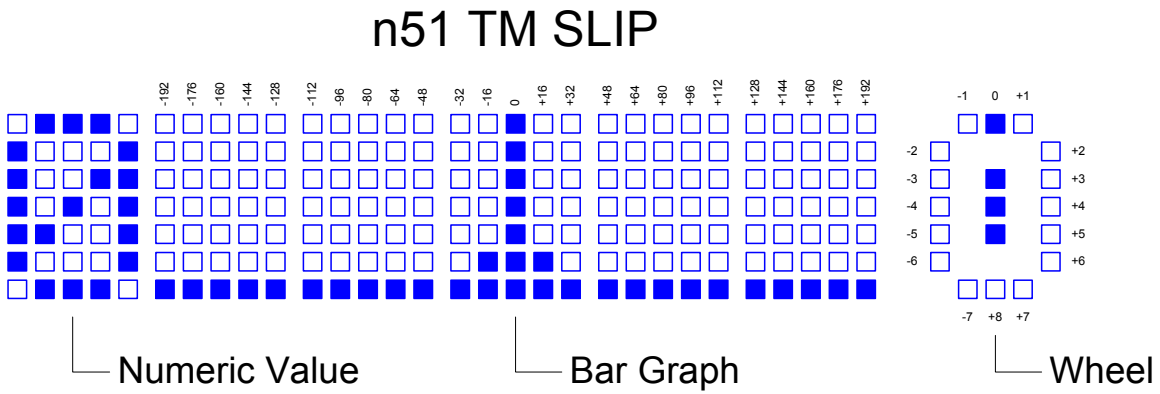
When measuring timing slips, a received DS-1 signal on Line 1 is compared to a reference DS-1 signal connected to either the reference input on Line 2 or to the side panel BNC connector. If a DS-1 clock reference is connected to the side panel BNC connector, timing slip analysis can be performed on both Line 1 and Line 2.

Note: The T-BERD 224 side panel BNC connector is an unbalanced 75 ohm interface. All DS-1 interfaces are balanced 100 ohm interfaces, so a Balun is required to properly connect the BNC to a DS-1 interface. A suitable Balun (75 ohm unbalanced:100 ohm balanced) is available from North Hills Signal Processing (http://www.northhills-sp.com), model 1310 (case BB).

The n51 TM SLIP (, where "n" indicates Line 1 or Line 2, as in 151 or 251) result is displayed above the **RESULTS I** or **RESULTS II** switches in three separate portions of the screen. See Fig. II-1:

- Numeric value – Counts 0 to 999. Represents the total number of frame slips that have occurred. One frame slip equals 193 bit-slips
- Bar graph - Represents partial frame slips in increments of one vertical bar for every 16 bit-slips. Each bar equals one wheel rotation. Each time the bar moves to the end of the graph, it is reset to the center and the frame slip count is incremented
- Moving "wheel" - Used along with the bar graph to display the direction, rate and number of bit-slips.

Figure II-1 – T-BERD 224 Timing Slip Display



The number of bit-slips is determined by adding the number indicated by the wheel position to the corresponding bar graph value. For example, if the bar graph value is +96 and the wheel value is –3, the number of bits slips is +96-3 = +93 bits. This indicates that 93

more clock cycles were received at the Line 1 RX test input than were received at the reference input (either Line 2 RX or BNC connector).

The displayed result depends on whether the signal is being received on Line 1 or Line 2 as shown in Table II-1.

Table II-1 – Configuration and Displayed Results

Input	Clock Reference	Displayed Results
L1	L2	Screen 151 (L1 vs. L2); Screen 251 will be unavailable
L1 & L2	BNC	Screen 151 (L1 vs. BNC) and Screen 251 (L2 vs. BNC)
L1	BNC	Screen 151 (L1 vs. BNC); Screen 251 will be unavailable
L2	BNC	Screen 251 (L2 vs. BNC); Screen 151 will be unavailable

Timing slip results vary according to the timing relationship between the test and clock reference signals:

- If the test and reference signals are perfectly synchronized, the timing slip count remains at 0, the bar graph remains at center, and the wheel remains at top-center.
- If the two signals are synchronized, but one signal has wander, the timing slip count remains at 0 but the bar graph and wheel moves to one side and then the other. The long-term average is 0.
- If the two signals are not synchronized, and the test signal frequency is higher than the reference signal, the wheel moves clockwise, the bar graph moves to the right, and the timing slip count increments every 193 bit-slips. When the frequency difference is more than a few Hertz, the **TIMING SLIP** count, bar graph, and wheel move very rapidly.
- If the two signals are not synchronized, and the test signal frequency is lower than the reference signal, the wheel moves counter-clockwise, the bar graph moves to the left, and the timing slip count increments every 193 bit-slips. When the frequency difference is more than a few Hertz, the **TIMING SLIP** count, bar graph, and wheel move very rapidly.

Note: When using Line 2 as the clock reference, the T-BERD 224 works in unexpected ways. When the **RESULTS I** or **RESULTS II** ***Blank*** switches are used to set the display to **SUMMARY** and **RESULTS OK** is displayed, it will not be possible to use the ***Arrowed*** switches to scroll to Screen 151. It is best to always set **RESULTS I** or **RESULTS II** to **SIGNAL** with the ***Blank*** switches and then use the ***Arrowed*** switches to find Screen 151.

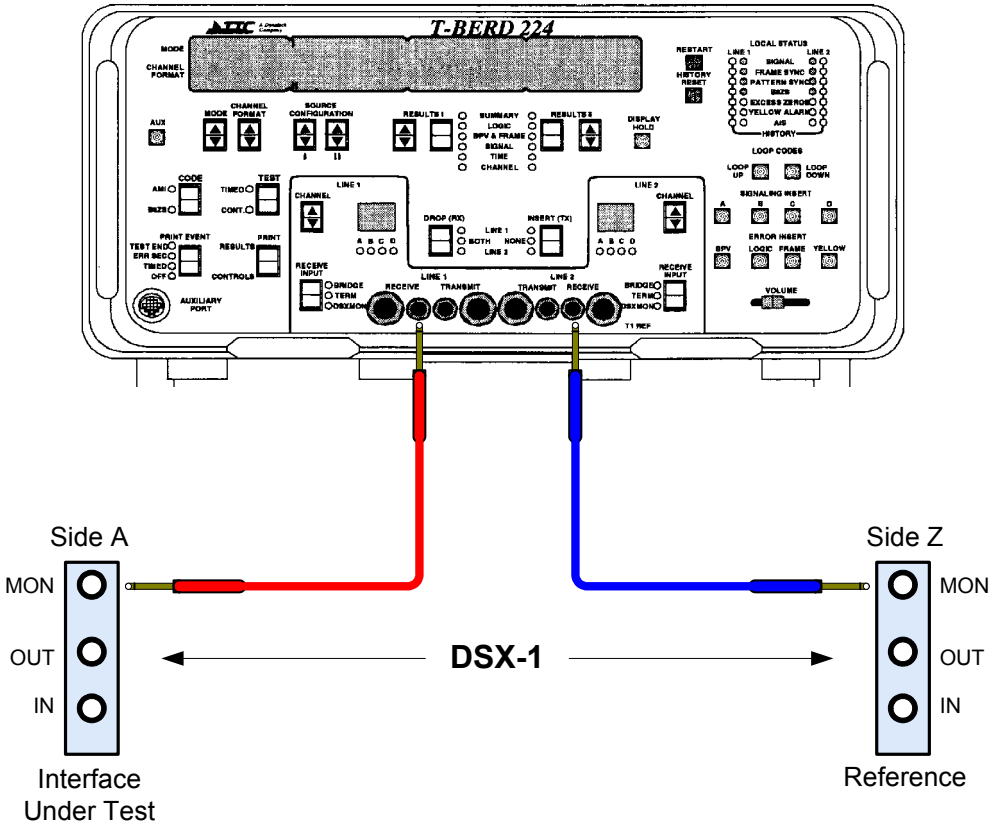
b. T-BERD 224 Configuration:

Step	Switch	Location	Action
1	**RESULTS I**	Middle, below screen	Select **SIGNAL** category using the ***Blank*** switch
2	**RESULTS II**	Middle, below screen	Select **SIGNAL** category using the ***Blank*** switch
3	**MODE**	Left, below screen	Select **AUTO** (or select the framing specified in the circuit order)
4	**SOURCE CONFIGURATION I**	Middle left, below screen	Select **AUTO**.
5	**CODE**	Far left	Select **B8ZS** or **AMI** as specified in the circuit order.
6	**TEST**	Left	Select **CONT**inous.
7	**PRINT EVENT**	Bottom left	Select **OFF**.
8	**DROP (RX)**	Middle lower, above jacks	Select **BOTH**.
9	**INSERT (TX)**	Middle lower, above jacks	Select **NONE**.
10	**Line 1 RECEIVE INPUT**	Left of test jacks	Select **DSX MON**.
11	**Line 2 RECEIVE INPUT**	Right of test jacks	Select **DSX MON**.

c. T-BERD 224 Connections:

Step	Action
1	Connect a patch cord from **Line 1 RX** jack to DSX-1 Side-A MON jack. See Fig. II-2.
2	Connect a patch cord from **Line 2 RX** jack to DSX-1 Side-Z MON jack. See Fig. II-2.
3	Press **RESTART** (Upper right, next to display).
4	Verify: a. **LINE 1 SIGNAL** and **LINE 2 SIGNAL** LEDs are illuminated. The LEDs are located on the upper right. b. **LINE 1 FRAME SYNC** and **LINE 2 FRAME SYNC** LEDs are illuminated. c. **MODE** display shows proper framing format (either **T1-D4** or **T1-ESF**). Do not proceed until the above has been verified.
5	Select screen 151 using the **RESULTS I** or **RESULTS II** ***Arrowed*** switches.

Figure II-2 – T-BERD 224 Connections



III – SunSet T10

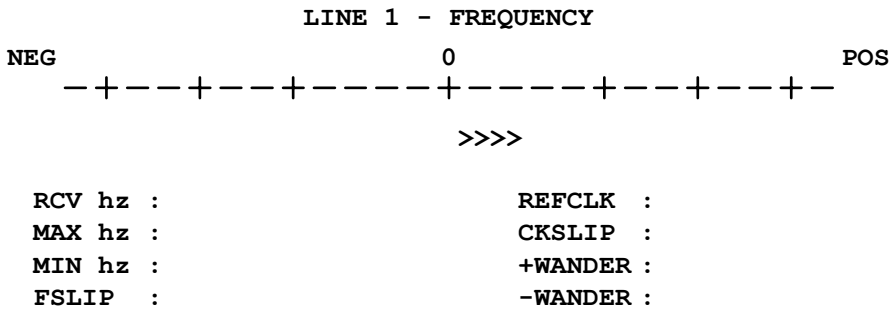
a. General:

When measuring timing slips, a received DS-1 signal connected to Line 1 is compared to a reference DS-1 signal connected to Line 2.

The relative timing measurement results are displayed on the **LINE 1 – FREQUENCY** screen. See Fig. III-1:

- **Bar graph** - Represents partial frame slips. The ">" or "<" symbol below the bar graph indicates the bit-slip direction, either Positive (">") or Negative ("<"). Each symbol represents 16 bit slips. If no symbol is displayed, there are no bit-slips. If the symbols are not moving, the number of bit-slips is not changing.
- **RCV hz** – Frequency of the signal on Line 1.
- **MAX hz** – Maximum frequency of the signal on Line 1 since the last **RESYNC**.
- **MIN hz** – Minimum frequency of the signal on Line 1 since the last **RESYNC**.
- **FSLIP** – Number of frame slips since the last **RESYNC**. This counter increments each time the **CLKSLIP** counter reaches 192 bit-slips. At that time the bar graph display is reset to center.
- **REFCLK** – Reference clock frequency source; always reads **L2-RX**.
- **CLKSLIP** – Number of bit-slips since the last **RESYNC**. This counter is the sum of the **+WANDER** and **–WANDER** counters. When the **CLKSLIP** counter reaches 192 bit-slips (**POS** or **NEG** extreme), the **FSLIP** counter is incremented.
- **+WANDER** – Number of bit-slips occurring in the positive direction.
- **–WANDER** – Number of bit-slips occurring in the negative direction.

Figure III-1 – Sunset T10 Timing Slip Display



The test set determines the number of bit-slips by adding the number indicated by **+WANDER** to the number indicated by **–WANDER**. For example, if the **+WANDER** value is +41 and the **–WANDER** value is 5, the number of bits slips is +41-5 = +36

bits. This indicates that 36 more clock cycles were received at the Line 1 RX test input than were received at the Line 2 RX reference input.

Timing slip results vary according to the timing relationship between the test and clock reference signals:

- If the test and reference signals are perfectly synchronized, the **CLKSLIP** count remains at 0 and the bar graph remains at center with no "<" or ">" symbols displayed.
- If the two signals are synchronized, but one signal has wander, the **CLKSLIP** count remains at 0 but the total of **+WANDER** and **–WANDER** will increase or decrease in equal amounts over time.
- If the two signals are not synchronized, and the test signal frequency is higher than the reference signal, the **CLKSLIP** counter increases, the symbols on the bar graph move to the right, and the **FSLIP** counter increments every 192 bit-slips. When the frequency difference is more than a few Hertz, the **CLKSLIP** count and bar graph move very rapidly.
- If the two signals are not synchronized, and the test signal frequency is lower than the reference signal, the **CLKSLIP** counter increases, the symbols on the bar graph move to the left, and the **FSLIP** counter increments every 192 bit-slips. When the frequency difference is more than a few Hertz, the **CLKSLIP** count and bar graph move very rapidly.

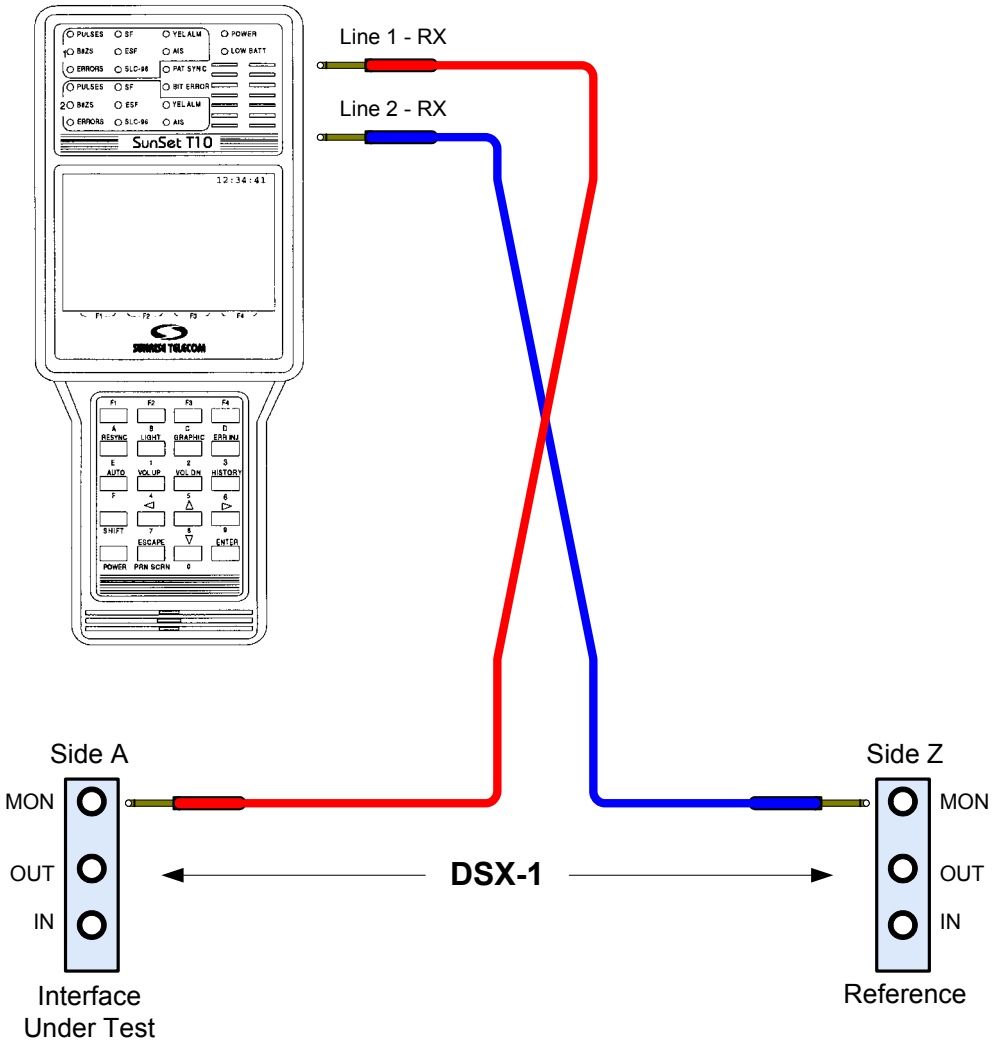
b. SunSet T10 Configuration:

Parameter	Setting	Remarks
TEST MODE	T1DUAL	Required setting
Tx/INSERT	L1-Tx	Not applicable to test
RX/DROP	L1-Rx	Not applicable to test
RxLVL-1	DSXMON	Required setting
RxLVL-2	DSXMON	Required setting
TxSOURCE	THRU	Not applicable to test
FRAMING	(As required)	Required setting; may be determined by pressing AUTO
CODING	(As required)	Required setting; may be determined by pressing AUTO
XMT CLOCK	L1-Rx	Not applicable to test
TEST RATE	1.544M	Required setting
LBO 1&2	0 dB	Not applicable to test

c. SunSet T10 Connections:

Step	Action
1	Connect a patch cord from **Line 1 RX** jack to DSX-1 Side-A MON jack. See Fig. III-2.
2	Connect a patch cord from **Line 2 RX** jack to DSX-1 Side-Z MON jack. See Fig. III-2.
3	Press **RESYNC**.
4	Verify: a. **Line 1 PULSES** and **Line 2 PULSES** LEDs are illuminated. b. **Line 1 SF** or **ESF** and **Line 2 SF** or **ESF** LEDs are illuminated, depending on Framing selected. c. **ERRORS** LED is off or, if flashing, press **HISTORY** key to stop flashing. Do not proceed until the above has been verified.
5	Press **ESCAPE**; use the cursor keys to select **MEASUREMENT RESULTS** and press **ENTER**.
6	Press **PgUp** (**F1**) one time to display **LINE 1 – FREQUENCY**.

Figure III-2 – SunSet T10 Connections

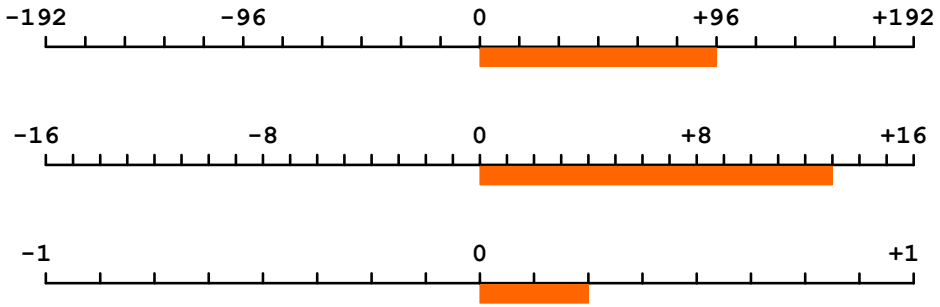


IV – HP 37702A

a. General:

The 37702A must be equipped with Option 001 Pulse Shape and Clock Slips and Wander Measurement. When measuring timing slips, a received DS-1 signal connected to the **T1 RECEIVE** is compared to the **TIMING REF DS1 INPUT**. The relative timing measurement results are displayed as a bar graph on the **SLIP/WANDER** screen under the **DISPLAY** menu. The display has very high resolution and is able to resolve 0.125 UI (Unit Interval), or 1/8 of a bit-slip. See Fig. IV-1:

Figure IV-1 – HP37702A Timing Slip Display



In addition to the bar graph, separate screens are available with counters that show the following. All wander counters are based on the Unit Interval, which is the length of a bit period at the signal rate (648 ns for a DS-1 signal):

UNCONTROLLED SLIPS (COFA)
CONTROLLED SLIPS
ESTIMATED FRAME SLIPS
ESTIMATED BIT SLIPS
POSITIVE PEAK WANDER
NEGATIVE PEAK WANDER
PEAK TO PEAK WANDER
TIME INTERVAL ERROR
PEAK TO PEAK 15 MINUTES
PEAK TO PEAK 24 HOURS

The test set determines the number of bit-slips by incrementing the **ESTIMATED BIT SLIPS** counter each time 1 UI is exceeded on the lower bar graph.

DS-1 Relative Timing Measurements

Timing slip results vary according to the timing relationship between the test and clock reference signals:

- If the test and reference signals are perfectly synchronized, the **ESTIMATED BIT SLIP** count remains at 0. The lower bar graph may indicate fractional UI wander. The **POSITIVE PEAK WANDER** and **NEGATIVE PEAK WANDER** will indicate fractional wander.
- If the two signals are synchronized, but one signal has wander, the **ESTIMATED BIT SLIP** count remains at 0 but the **POSITIVE PEAK WANDER** and **NEGATIVE PEAK WANDER** will indicate wander to some extent. Both will increase or decrease in equal amounts over time.
- If the two signals are not synchronized, and the test signal frequency is higher than the reference signal, the **ESTIMATED BIT SLIP** counter increases, the symbols on the bar graph move to the right, and the **CONTROLLED SLIPS** and **ESTIMATED FRAME SLIPS** counter increments every 192 bit-slips. When the frequency difference is more than a few Hertz, the **ESTIMATED BIT SLIP** count and bar graph move very rapidly.
- If the two signals are not synchronized, and the test signal frequency is lower than the reference signal, the **ESTIMATED BIT SLIP** counter increases, the symbols on the bar graph move to the left, and the **CONTROLLED SLIPS** and **ESTIMATED FRAME SLIPS** counter increments every 192 bit-slips. When the frequency difference is more than a few Hertz, the **ESTIMATED BIT SLIP** count and bar graph move very rapidly.
- If there are uncontrolled frame slips (change of frame alignment, COFA, occurs), the **UNCONTROLLED SLIPS** counter will increase.

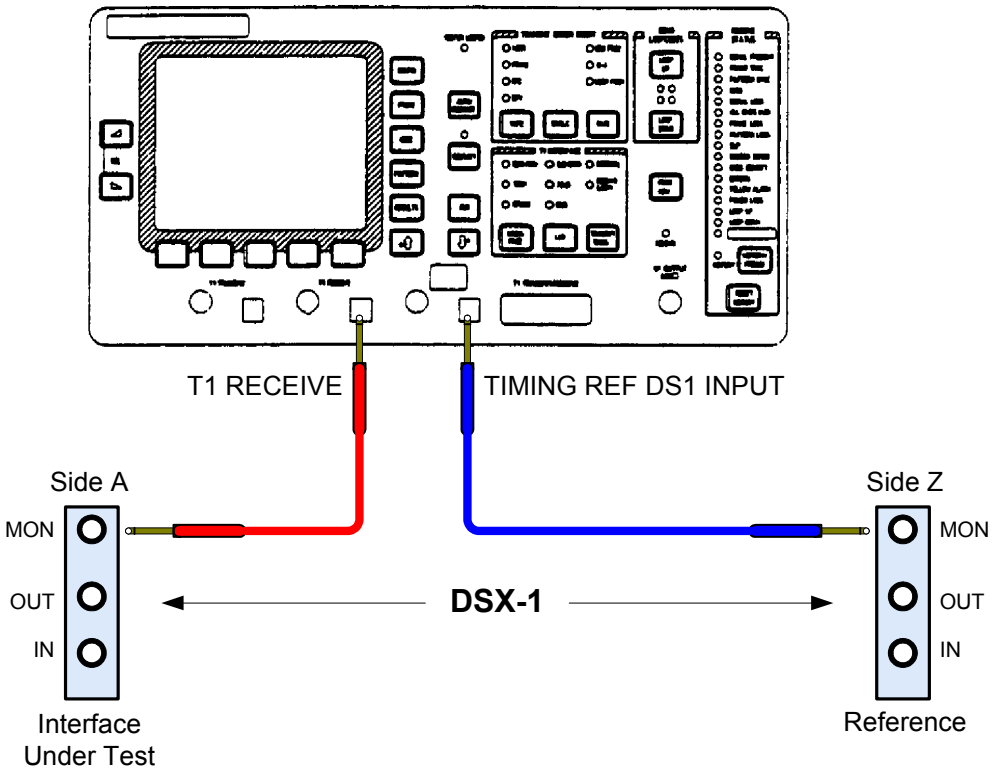
b. HP37702A Configuration:

Step	Button	Location	Action
1	**CONFIG**	Right of screen	Select **Full T1** using the ***Status*** switches below the screen
2	**FRAME**	Right of screen	Select **D4** or **ESF** category, as specified in the circuit order, using the ***Status*** switches below the screen
3	**CODE**	Right of screen	Select **AMI** or **B8ZS**, as specified in the circuit order
4	**PATTERN**	Right of screen	Use cursor key to move one field to the left and then select **MULTI** or **PATTERN** using the ***Status*** switches below the screen
5	**INTERFACE**	Lower middle	Select **DSX-MON**
6	**CODE**	Far left	Select **B8ZS** or **AMI** as specified in the circuit order.

c. HP37702A Connections:

Step	Action
1	Connect a patch cord from **T1 RECEIVE** jack to DSX-1 Side-A MON jack. See Fig. IV-2.
2	Connect a patch cord from **TIMING REF DS1 INPUT** jack to DSX-1 Side-Z MON jack. See Fig. IV-2.
3	Press **RESTART**.
4	Verify: a. **SIGNAL PRESENT** and **FRAME SYNC** LEDs are illuminated. The LEDs are located on the upper right. b. No errors indicated by the Red LEDs. c. If **HISTORY** LED is illuminated, press **RESET HISTORY**. Do not proceed until the above has been verified.
5	Press **RESULTS** button located to lower right of screen. Use the cursor buttons to move the cursor to the first **DISPLAY** field in the upper middle of the screen.
6	Press the **MORE *Status*** button below the screen. On the second screen press the **SLIPS/WANDER** button.
7	Use the cursor keys to move the screen cursor to the second **DISPLAY** field on the screen. At the bottom of the screen, use the ***Status*** buttons to select **SLIPS**, **WANDER**, **GRAPH**.

Figure IV-2 – HP37702A Connections



V - TTC T-BERD 2209

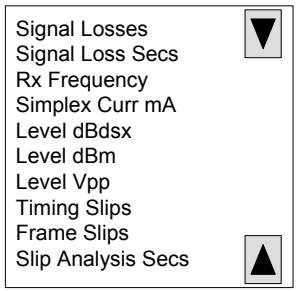
a. General:

When measuring timing slips with the TTC 2209 Test Pad, a received DS-1 signal on the Primary Receive port is compared to a reference DS-1 signal connected to the Secondary Receive port.[1] Measurements can be made with test pad application modules configured either for DS1 or DS3.

The TTC 2209 does not provide a graphical display of timing and frame slips. Instead, it displays the number of **Timing Slips**, **Frame Slips** and **Slip Analysis Seconds** as shown in Fig. V-1:

- **Timing Slips** – Counts 0 to 193. Represents the total number of bit (clock) slips that have occurred. Each time the number of timing slips counts past 193, the **Timing Slips** counter is reset to zero and the **Frame Slips** counter is incremented by one count.
- **Frame Slips** – Counts the total number of frame slips that have occurred. One frame slip equals 193 bit-slips.
- **Slip Analysis Seconds** – Counts the number of seconds since the last **Restart**.

Figure V-1 – T-BERD 2209 Slip Counters (bottom three measurement parameters)



Timing slip results vary according to the timing relationship between the test and clock reference signals:

- If the test and reference signals are perfectly synchronized, the **Timing Slips** count remains at 0.
- If the two signals are synchronized, but one signal has wander, the **Timing Slips** count may temporarily increase and then decrease. The long-term average is 0.
- If the two signals are not synchronized, and the test signal frequency is lower or higher than the reference signal, the **Timing Slips** count increments and the **Frame Slips** count increments every 193 bit-slips. When the frequency difference is more than a few Hertz, the **Timing Slips** count moves very rapidly.

[1] Actually, since this is a relative timing measurement, either port can be used for the reference. It is only necessary that one DS1 be a known good timing source to ensure useful measurement results.

b. T-BERD 2209 Configuration:

Step	Soft Switch	Location	Action
1	**Application Buttons**	Upper Left windowpane	Tap **MON**
2	**Drop Down Menu**	Below Application Buttons	Tap **Monitor T1**
3	**Drop Down Menu**	To Right of previous menu	Tap **T1 External**
4	**Setup Button**	Upper Right windowpane	Tap **Setup**
5	**Tx Coding Radio Button**	Right side of windowpane	Select **B8ZS** or **AMI** as specified in the circuit order.
6	**Framing Radio Button**	Left side of windowpane	Select **Auto Framing**
7	**OK Button**	Bottom Left of windowpane	Tap **OK**
8	**Left Result Group Button**	Middle-Left windowpane	Tap **Primary**
9	**Right Result Group Button**	Middle-Right windowpane	Tap **Secondary**
10	**Left Result Category Button**	Middle-Left windowpane	Tap **Summary**
11	**Right Result Category Button**	Middle-Right windowpane	Tap **Summary**

c. T-BERD 2209 Connections:

Step	Action
1	Connect a patch cord from **Primary Receive** jack to DSX-1 Side-A MON jack. See Fig. V-2.
2	Connect a patch cord from **Secondary Receive** jack to DSX-1 Side-Z MON jack. See Fig. V-2.
3	Press **RESTART** (Upper right, next to display)
4	Verify: a. **Primary SIGNAL** and **Secondary SIGNAL** LEDs are green. The LEDs are located just below the receive jacks. b. **Primary FRAME** and **Secondary FRAME** LEDs are green. The LEDs are located just below the transmit jacks. c. **RESULTS OK** shows in both **Results Category** windowpanes. Do not proceed until the above has been verified.
5	Select **Timing Slips** in **Left Result Category** and **Frame Slips** in the **Right Result Category**.

Figure V-2 – T-BERD 2209 Connections