Telecommunications Synchronization Overview

1. Introduction

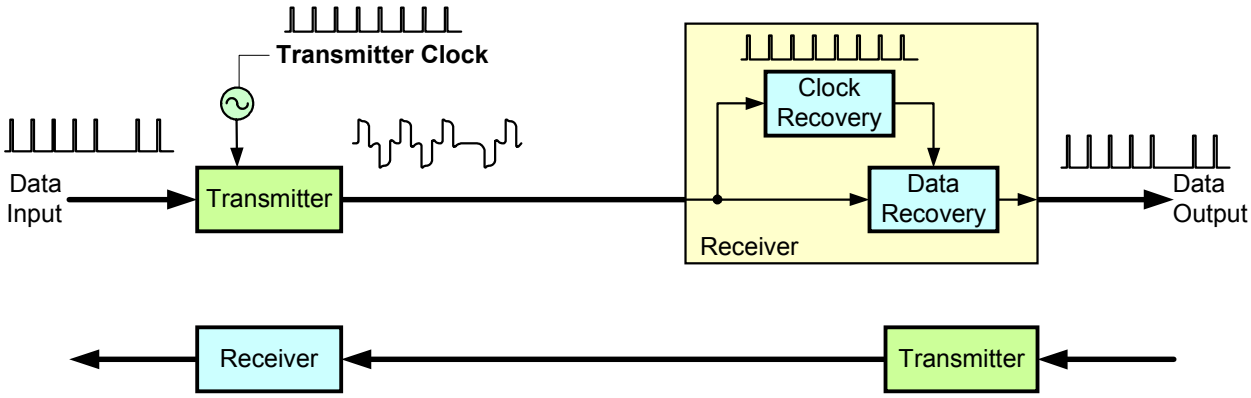
The introduction of digital 64 kb/s circuit switches (end office and tandem switching systems) and digital cross-connect systems in the late 1970s and early 1980s drove the need for network synchronization.

Synchronization in telecommunications networks is the process of aligning the time scales of transmission and switching equipment so equipment operations occur at the correct time and in the correct order. Synchronization requires the receiver clock to acquire and track the periodic timing information in a transmitted signal.

The transmitted signal (Fig. 1a) consists of data that is clocked out at a rate determined by the transmitter clock. Signal transitions between zero and peak values contain the clocking information and detecting these transitions allows the clock to be recovered at the receiver (Fig. 1b). The recovered clock is used to write the received data into a buffer, also called elastic store or circular shift register, to reduce jitter (jitter is discussed later in this section). The data is then read out of the buffer onto a digital bus for further multiplexing or switching (Fig. 1c).

Fig. 1a – Transmitter and Receiver Clocks

The received signal is processed by the clock recovery circuit, and the clock is then used to recover the data. The transmitter and receiver circuits for both directions are identical. The receiver on the right is shown in slightly more detail.



All problems in digital networks, including poor synchronization, are manifested as errors. Examples of the results of poor synchronization are

- Degraded speech quality and audible clicks
- Degraded data traffic throughput
- Call setup, takedown, and management problems
- Corrupt or incomplete fax messages
- Low dialup modem speeds
- Freeze-frames and audio pops on video transmissions
- Call disconnects during mobile call hand-off
- Partial or complete traffic stoppage

Fig. 1b – Clock Recovery

The incoming bipolar signal (typical of baseband digital transmission systems) is sliced at a consistent point on the signal waveform, 50% of peak in this example. Timing is recovered from the sliced waveform edges and is used to recovery the data. The recovered timing is one input to a phase detector and the output of a voltage-controlled oscillator (VCO) is used as the other input to the phase detector. The output of the phase detector is a dc voltage that is proportional to the phase difference. This output is filtered and used to adjust the output frequency of the VCO. In this way, the VCO tracks the phase of the input signal clock. This combination of a phase detector, filter and VCO is called a Phase Locked Loop (PLL) and is used as the equipment clock.

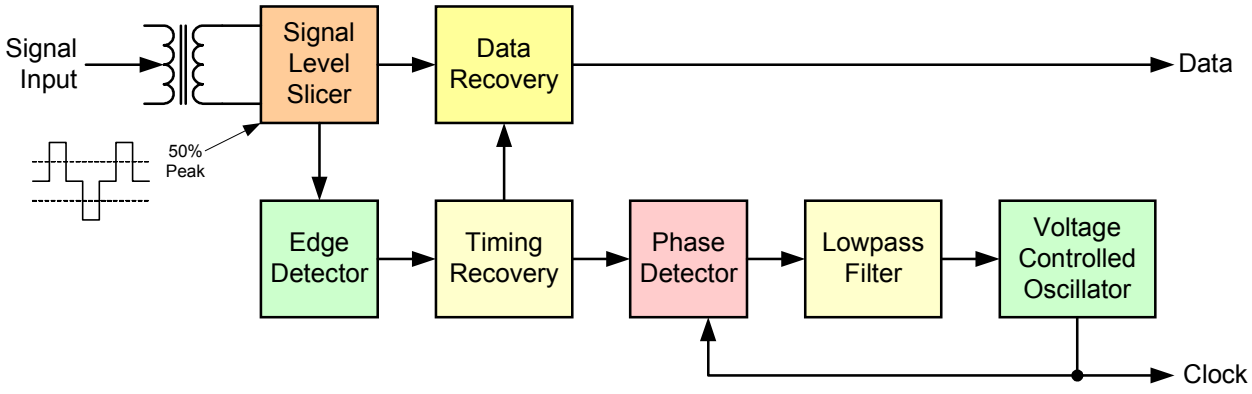
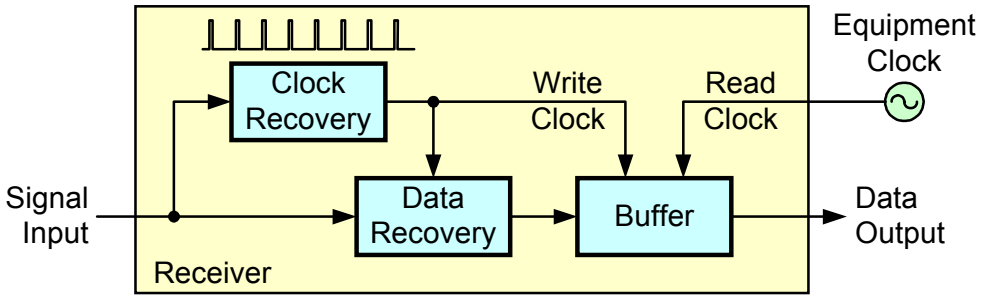


Fig. 1c – Data Buffering

The buffer allows the recovered clock (write clock) and the equipment clock (read clock) to have slightly different frequency or phase. In loop-timed equipment, the write clock also drives the read clock to make them exactly the same.



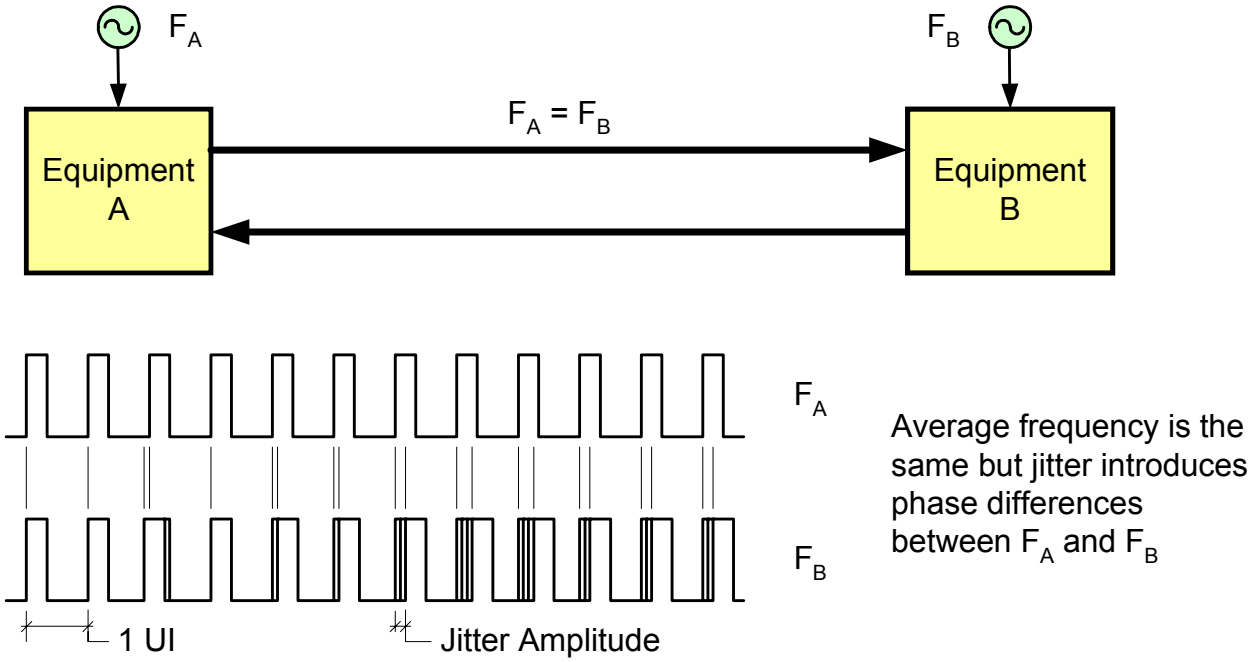
Buffer sizes vary from 386 bits (two DS-1 data frames) to 4,632 bits (two DS-1 SuperFrames) or 9,264 bits (two DS-1 Extended SuperFrames).[1] The larger buffers are used to minimize multiplexer recovery time upon loss of framing. Buffer size always is twice the data block size to allow the buffer start at the center and then move either way.

In an ideal transmission system, signal pulses are transmitted at precise intervals (pulse repetition period) and arrive at the receiver with exactly the same time spacing. In real systems, the signals are transmitted at a rate determined by an imperfect clock and arrive at slightly different times due to physical and electrical transmission processes. The received signals may be corrupted by noise, subjected to phase delay distortion and detected by imperfect clock recovery circuits. All of these problems result in jitter and wander, which is any kind of phase noise or fluctuations of

[1] SuperFrame is commonly known as SF or D3/D4 or just D3 or just D4; all terms are interchangeable. Extended SuperFrame is commonly known as ESF.

the recovered timing signals along the time axis (Fig. 2). Jitter is defined as phase variations that occur at a rate greater than 10 Hz and wander occurs at a rate less than 10 Hz.

Fig. 2 – Phase Noise on a Timing Signal Results in Jitter and Wander
The transmitter clock, F_A, shown in this example is jitter-free, but as a result of phase noise, the recovered clock, F_B, at the receiver contains jitter and wander.



Jitter is due to multiplexing processes, clock circuit design and the effects of amplitude and phase noise. Wander is due to pointer justifications (movement) in synchronous optical networks (SONET) and physical processes such as temperature variations. In the case of geostationary communications satellite circuits, wander is due to the motion of the satellite in its orbit. Very low rate wander in terrestrial communications facilities is caused by the expansion and contraction of cables from diurnal and seasonal heating and cooling effects and by the varying propagation conditions along microwave radio paths. Wander, particularly very low rate wander, is impossible to eliminate.

High synchronization quality is achieved by the application of

- Very accurate and stable oscillators (clocks) to control the time scales
- Buffers to control the inevitable slight differences in frequency and to minimize the effects of jitter and wander.

There is no such thing as a perfect clock or a set of network equipment clocks that all operate at exactly the same frequency and that have the same stability characteristics. Buffers temporarily overcome slight frequency differences (offset) and absorb jitter and wander. However, any sustained frequency offset between clocks or excessive jitter and wander amplitudes cause buffer overflow or underflow. Overflow leads to the deletion of a block of bits in the buffer and underflow leads to repetition of a block of bits in the buffer (data bits are deleted or repeated by changing the buffer read pointer address).

The deletion and repetition of a data block is called a slip. If the block consists of only one bit, it is called a bit slip or clock slip. If the block consists of an entire data frame (for example, the 192 payload bits in a DS1 frame), it is called a frame slip. If the slip occurs at the frame boundary and the framing bit is not lost, it is called a *controlled slip*. On the other hand, an *uncontrolled slip* means that identification of the frame boundary was lost and there was a Change Of Frame Alignment (COFA). An uncontrolled slip is more serious because meaningful transmission is interrupted (the receiver is unable to accurately read bit values) until framing is re-established.

The overall object of network synchronization is to minimize controlled slips and eliminate uncontrolled slips. This can be achieved only by synchronizing all equipment clocks in all nodes to the same master clock or to a number of master clocks that operate plesiochronously (very closely matched).

Frame slips have different effects on different traffic types. Table 1 shows the effects of a single frame slip on an individual 64 kb/s (DS-0) channel. The slip rate between plesiochronous networks can be calculated from Eq. 1.

$$SR = \Delta f \cdot FR \cdot 86{,}400 \qquad \text{Eq. 1}$$

where

SR =	Slip rate (frame slips/day)
Δf =	Frequency accuracy difference
FR =	Frame rate (frames/second) [Note: All telecommunications systems operate at 8,000 frames/second]
86,400 =	Number of seconds/day

As an example, consider two networks that are synchronized by different clocks. One clock has an accuracy of $+1 \times 10^{-11}$ and the other has an accuracy of -1×10^{-11}. The accuracy difference in this case is 2×10^{-11}. Therefore, the slip rate is 2×10^{-11} x 8,000 frames/second x 86,400 seconds/day = 0.0138 frame slips/day, or 72.3 days/frame slip.

Table 1 – Effects of Single Frame Slip

Service	Effects
Voice, PCM Coding	No effect during silent periods; otherwise, audible click
Voice, Compressed	Depends on compression method but is much worse than uncompressed PCM voice
Encrypted Voice or Data	Loss of voice or data transmission; retransmission of encryption key
Program Voice or Music	Audible click
Facsimile	Corruption of 8-10 scan lines or dropped call
Video	Picture outage or freeze-frame for several seconds; loud “pop” on audio; low bit-rate (compressed) video affected more than high bit-rate
Digital Data	Block retransmission; deletion or repetition of data
Voiceband Data	Carrier drop-out or error burst lasting 10 milliseconds to 1.5 seconds

2. Clock Types

Telecommunications clock performance is specified according to the synchronization hierarchy, or clock stratum level, defined in ANSI T1.101 (Table 2). The slip rate in this table is based on the assumption that one of the clocks is a Stratum 1 clock operating at its maximum positive or negative offset and the other clock is the stratum level specified and is operating at its maximum offset opposite of the Stratum 1 clock.

Table 2 – ANSI T1.101 Clock Performance Requirements

Stratum Level	Free-Run Accuracy	Holdover Accuracy in 1st 24 Hours	Slip Rate @ DS-1 Rate	Rearrangement MTIE
1	$1x10^{-11}$	N/A	≤1 Slip in 72 days	N/A
2	$1.6x10^{-8}$	$1x10^{-10}$	≤1 Slip in 13 days	1 μs
3E	$4.6x10^{-6}$	$1x10^{-8}$	≤7 Slips in 1 day	1 μs
3	$4.6x10^{-6}$	$3.7x10^{-7}$	≤255 Slips in 1 day	1 μs
4	$32x10^{-6}$	N/A	N/A	1 μs

The highest performance clock is Stratum 1, often also called a Primary Reference Source (PRS). A Stratum 1 clock and PRS are not the same but both have the same accuracy and the terms often are used interchangeably. A Stratum 1 clock, by definition, is autonomous, whereas a PRS can be either autonomous or not. In any case, the PRS must be traceable to a Stratum 1. A PRS based on GPS or LORAN-C is not autonomous but it does meet the traceability requirement. A Cesium beam clock is the only autonomous clock used in telecommunication applications, so it is the only PRS that meets the Stratum 1 definition.

Stratum 1 provides adequate slip performance between plesiochronous networks. If two interconnected networks are each independently synchronized by Stratum 1 clocks, one operating at its minimum specified frequency and the other operating at its maximum specified frequency, there will be no more than 1 frame slip in 72 days.

Presently, there are two basic categories and three basic types of PRSs in common use

- Autonomous
  - Quartz crystal oscillator controlled by a Cesium beam oscillator
- Radio controlled
  - Quartz crystal oscillator controlled by a GPS receiver
  - Quartz crystal oscillator controlled by a LORAN-C receiver

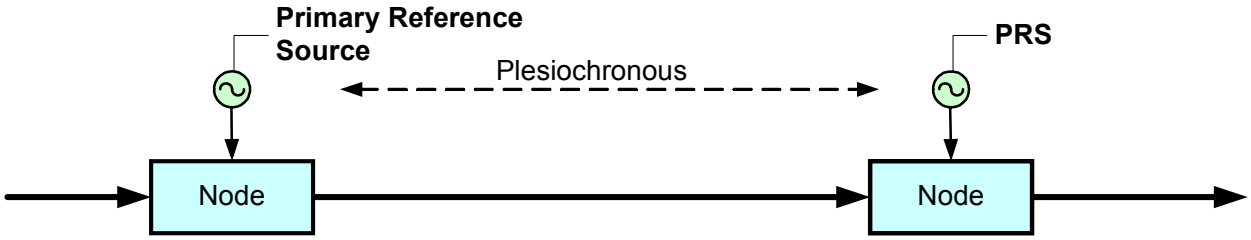
The long-term accuracy of all GPS and LORAN-C receiver oscillators is ultimately traceable to Universal Coordinated Time (UTC), which is based on ensembles of Cesium beam oscillators. It should be noted that Cesium beam oscillators, GPS receivers and LORAN-C receivers by themselves do not have the necessary short-term stability, so they depend on ovenized quartz crystal oscillators (OCXO), which perform well over the short-term. Presently, GPS receivers are the most common PRS.

Stratum 1 and 2 clocks generally are used in Synchronization Supply Units (SSU) that provide timing distribution to all network equipment in a building.[2] In this application, the Stratum 2 clocks are used for holdover when the Stratum 1 clock fails. Stratum 2 clocks sometimes are found in end office and transit circuit-switching systems, but these systems usually are equipped with Stratum 3 clocks. The Stratum 3E clock is used in SONET network elements (called SONET Equipment Clock, SEC, or SONET Minimum Clock, SMC), and the Stratum 4 clock is used in primary multiplexers (channel banks), digital loop carrier terminals and similar equipment. Some local area network equipment, such as routers, and customer premises private branch exchanges may be equipped with Stratum 4 clocks; however, this equipment most often does not meet any of the ANSI T1.101 requirements.

3. Synchronization Methods

The very high quality PRS timing reference is used to provide a timing source for local network equipment (Fig. 3a) or it can be transported to all network elements that require synchronization using the master-slave method (Fig. 3b). When a PRS is located at each network node, the network equipment operates plesiochronously. Most PRSs are controlled by GPS receivers and ultimately timed by the same set of satellites. In this case, the networks are said to operate pseudo-synchronously. The master-slave method frequently is used in SONET networks (Fig. 4).

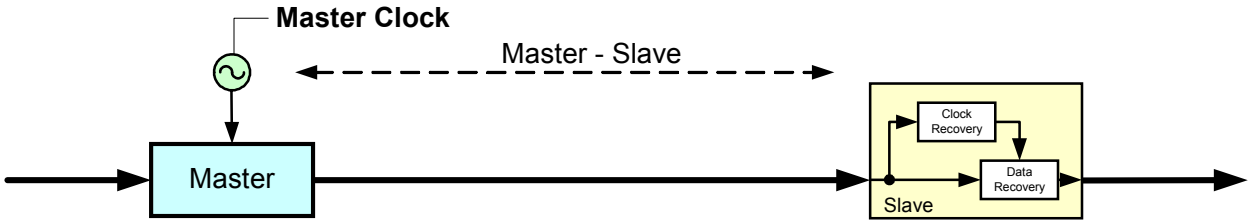
Fig. 3a – Plesiochronous Operation



- The two Primary Reference Sources have nearly the same frequency so there is little difference between the transmit and receive rates
- Slip rate is very low (< 1 slip in 72 days)

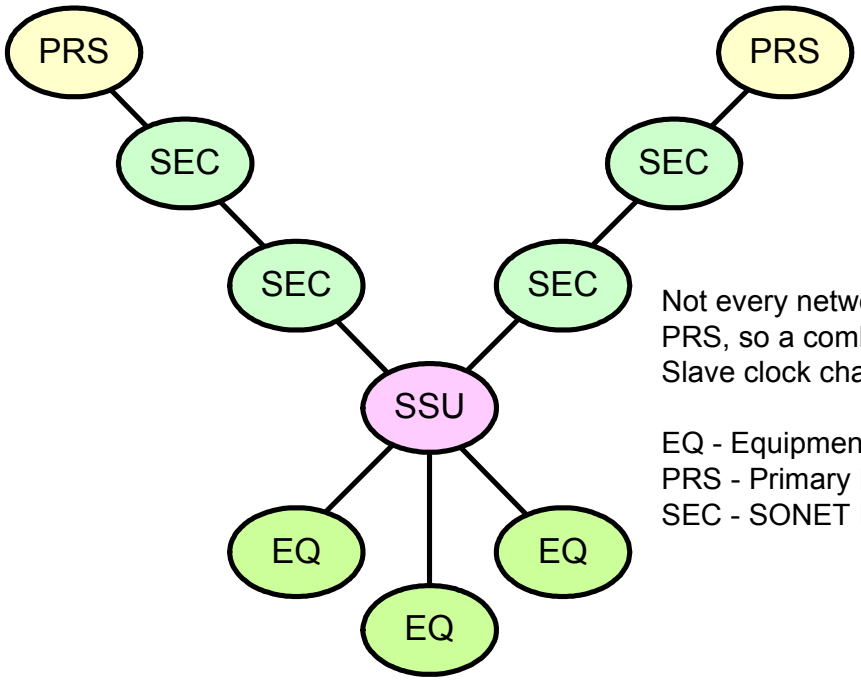
[2] The contemporary name in North America for an SSU is Building Integrated Timing Supply (BITS), but use of the term BITS is falling out of favor as industry standards are harmonized with international recommendations.

Fig. 3b – Master-Slave Operation



- The slave clock continuously adjusts to incoming signal frequency
- Master-Slave clocks have the same frequency so there are no slips

Fig. 4 – Synchronization Chain Using Master-Slave Connected Clocks



Not every network node is connected to a PRS, so a combinations of PRS and Master-Slave clock chains are used

EQ - Equipment
PRS - Primary Reference Source
SEC - SONET Equipment Clock

Telecommunications clocks (except Cesium beam PRSs) operate in three modes

- Normal mode (locked to input reference)
- Holdover
- Free-run

Depending on their position in the synchronization hierarchy, equipment clocks have different accuracies for each mode. When an equipment clock is operating in Normal mode, its accuracy is equal to the accuracy of its reference. That is, the clock is *traceable* to a Stratum 1 clock source and has the long-term accuracy of the PRS. When it is in the Normal mode, the clock's short-term performance depends on the quality of its clock recovery circuit, internal oscillator, and jitter and wander filter.

A clock in Holdover mode has previously operated in Normal mode but has lost its input reference and is using stored data (acquired during Normal mode) to control its output frequency and phase. Holdover ends when the clock once again operates in the Normal mode. The clock output frequency will not change suddenly during the transition from Normal to Holdover mode, but it will slowly drift away as the oscillator is affected by its physical environment and aging effects. A well-designed clock does not introduce large phase jumps during the transition to and from Holdover mode.

A clock in Free-run mode has never operated in the Normal mode, has lost stored data associated with Holdover mode, or has been in Holdover for more than several days or weeks. Free-run mode ends when the clock acquires and tracks its input reference. A clock in Free-run mode will drift and eventually will operate at its maximum frequency offset. A PRS essentially operates in Free-run mode but not necessarily at its maximum frequency offset.

Different network elements have different clock performance requirements while in holdover to achieve a suitable trade-off between cost and slip performance. Ideally, every network element would be equipped with a PRS, but this is not economically feasible.

As previously mentioned, during normal operation an equipment clock takes on the accuracy of its reference source. When the reference input is lost due to inevitable equipment or operational failures, the equipment clock changes to holdover mode. At this time, the slip performance of the affected network equipment depends on its holdover accuracy. For example, if a Stratum 3 clock uses a Stratum 2 clock as its reference, and the Stratum 2 clock, in turn, uses a PRS as its reference, the Stratum 3 clock will have Stratum 1 accuracy during normal operation. If the Stratum 2 clock loses its reference, then the Stratum 2 clock goes into holdover mode. The Stratum 3 clock still will be operating in normal mode but will have Stratum 2 accuracy. If the Stratum 3 clock loses its reference, it will go into holdover mode and will have Stratum 3 accuracy.

The lower the stratum level (higher the stratum number), the lower the clock's performance and the lower the holdover accuracy. For example, a Stratum 3 clock has lower performance than a Stratum 2 clock.

Clock performance can be broadly categorized as

- Accurate and stable (Fig. 5a)
- Accurate and unstable (Fig. 5b)
- Inaccurate and stable (Fig. 5c)
- Inaccurate and unstable (Fig. 5d)

Fig. 5a – Accurate and Stable Clock Performance

Fig. 5b – Accurate and Unstable Clock Performance

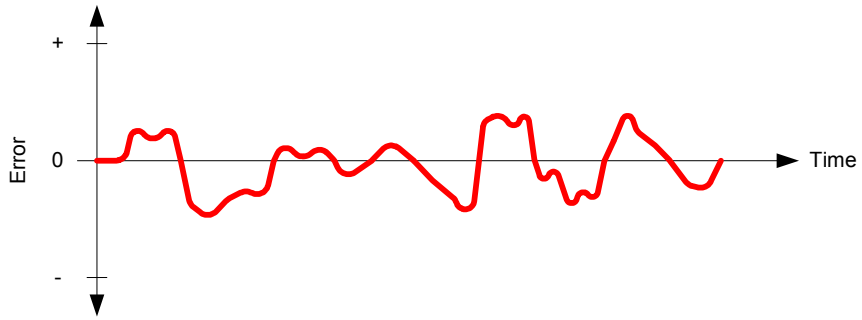


Fig. 5c – Inaccurate and Stable Clock Performance

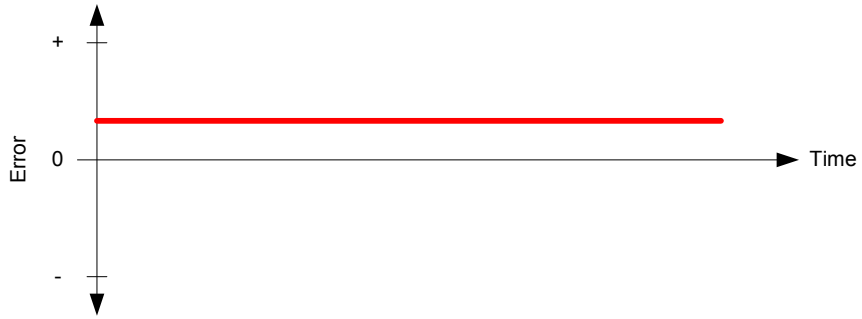
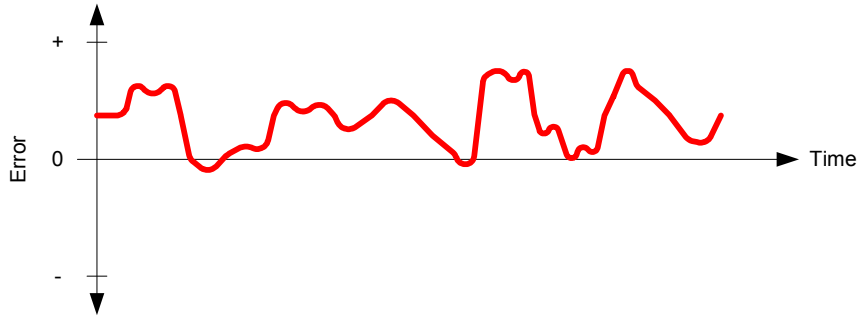


Fig. 5d – Inaccurate and Unstable Clock Performance



4. Timing Impairments

Jitter and Wander already have been described as any kind of phase noise or fluctuations of the recovered timing signal along the time axis. The phase noise can be generated by the transmission system, in the clock recovery circuits of an interface, and at the outputs of synchronization supply units (SSU).

Jitter and wander is described in time units such as seconds (seconds, microseconds, nanoseconds, picoseconds), phase angle (radians) or unit interval (UI). The most common unit is the Unit Interval, which is equal to the pulse period (reciprocal of the interface bit rate). For example, 1 UI at the DS-1 rate corresponds to (1 ÷ 1,544,000 b/s) 648 ns; therefore, a peak-to-peak jitter of 0.1 UI at a DS-1 interface is the same as 64.8 ns.

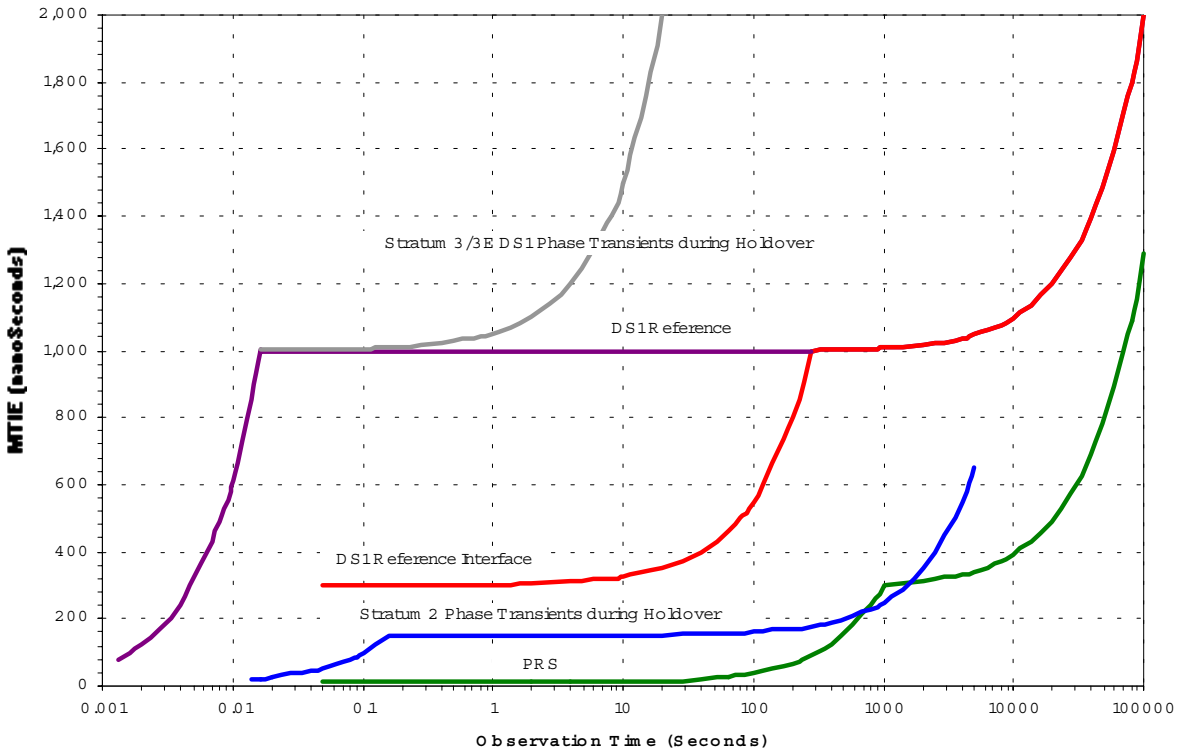
Jitter tolerance requirements that apply to the input of Stratum 2, 3E, 3 and 4 clocks are given in ANSI T1.102. A DS-1 timing output interface shall not generate more than 0.05 UI peak-to-peak jitter (per ANSI T1.101 Annex G).

The effect of transmission cables on wander is in the order of

- ~ 80 ps/km/°C for fiber optic cables
- ~ 725 ps/km/°C for metallic twisted pair cables

Time Interval Error (TIE) is the variation in time delay of a timing signal over a particular observation period relative to an ideal timing signal (or a very high quality reference signal). If the timing signal has a fixed frequency offset, the TIE will increase linearly over time with no upper bound – the longer the observation period the higher the TIE. If the timing signal phase delay varies during the observation period it will have some maximum value, or Maximum TIE (MTIE), during that period. MTIE is specified to ensure that slip performance is properly bounded particularly during loss and rearrangement of reference timing sources (Fig. 6).

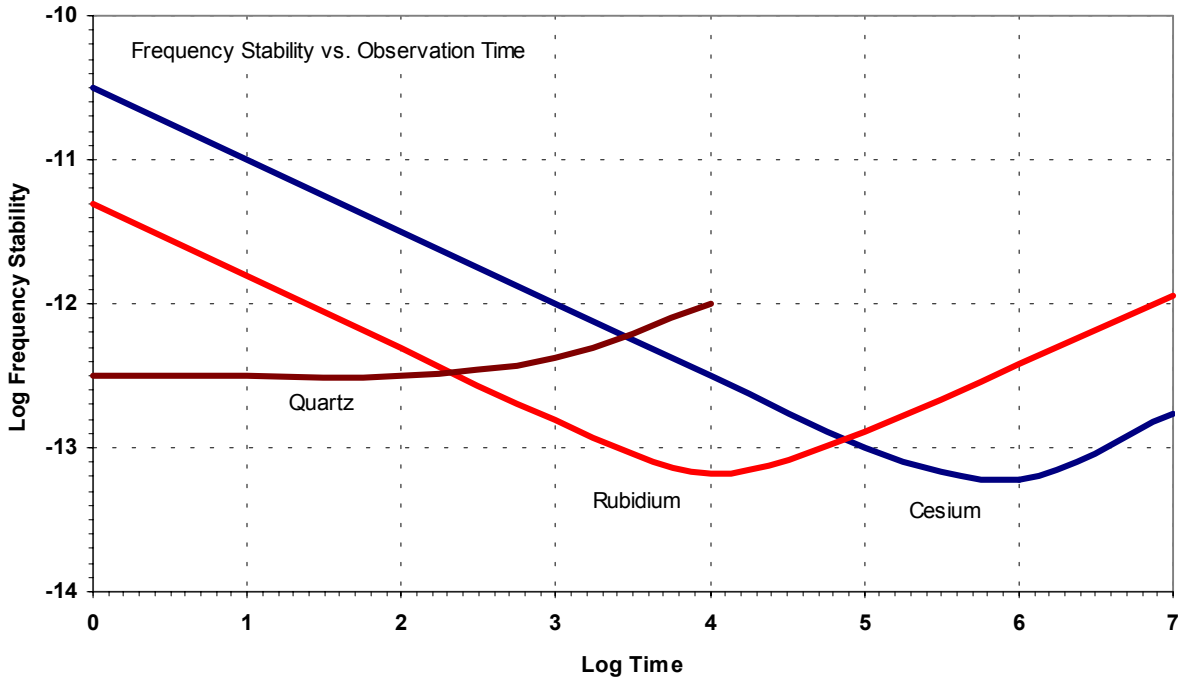
Fig. 6 – Maximum Time Interval Error (MTIE) vs. Observation Period



Time Deviation (TDEV) is a measure of the expected time variation of a timing signal as a function of integration time. It provides information about the spectral content of the timing signal's phase noise. It is calculated from a sequence of time error samples and is expressed in time units (usually nanoseconds). A constant frequency offset does not affect TDEV. In the case of linear frequency drift (linear increase in frequency offset), TDEV is proportional to the square of the observation period. TDEV gives more information on timing signal noise than MTIE.

MTIE and TDEV are specified as a function of measurement (observation) period because clocks have different observed behavior depending on the observation period. As previously mentioned, the output circuits of all telecommunications clocks use high quality quartz crystal oscillators to provide short-term stability. Crystal oscillators age and drift over time and are sensitive to temperature variations so they are steered by atomic clock generators (cesium or rubidium), which have very good long-term stability but relatively poor short-term stability. The combination of a high quality crystal oscillator and atomic clock generator provides the necessary stability over all observation periods (Fig. 7).

Fig. 7 – Clock Frequency Stability vs. Observation Period
This graph shows the log (base 10) frequency stability on the vertical scale. For example, a value of –12 represents a stability of 10^{-12}. Of the clocks shown, a Cesium oscillator has better stability for observation periods greater than 10^5 seconds (shown as 5 on the Log Time scale), or about 24 hours. The Rubidium oscillator provides better stability during intermediate periods from about 300 seconds to approximately 24 hours. The quartz crystal oscillator is better for observation periods less than 300 seconds. This graph illustrates why all high-accuracy oscillators use a combination of quartz crystal and atomic oscillators and why Cesium is used in Stratum 1 clocks and Rubidium usually is used in Stratum 2 holdover clocks.

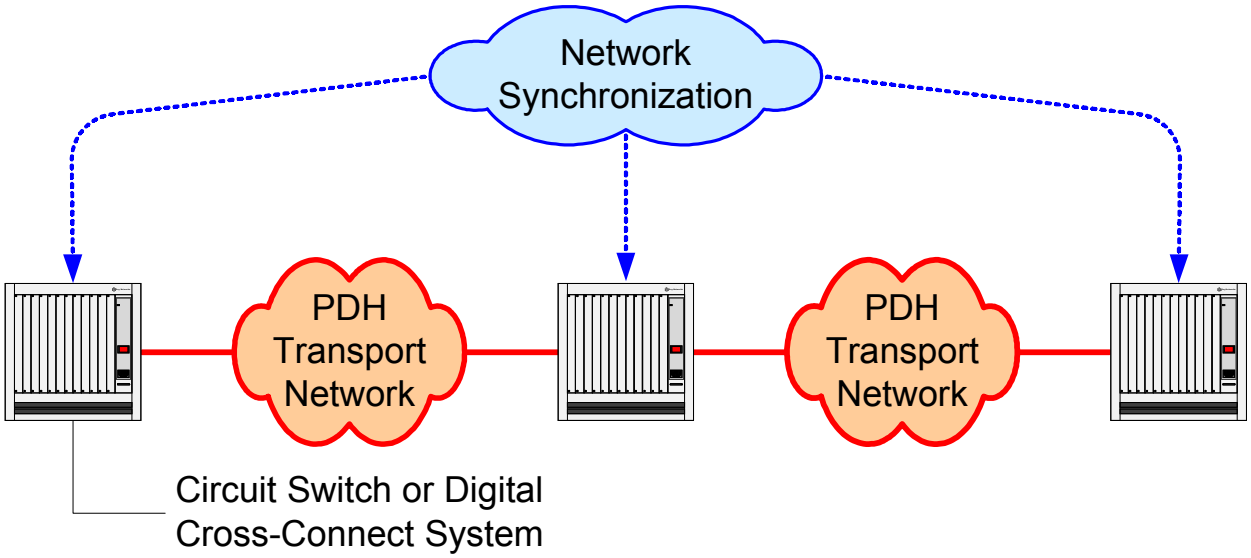


5. Synchronization Requirements in PDH and SONET Networks

Transmission and multiplex networks in common use today are built on the *Plesiochronous Digital Hierarchy* (PDH, also called the *electrical digital hierarchy*), the *Synchronous Digital Hierarchy* (SDH, or Synchronous Optical Network – *SONET, or optical digital hierarchy*), or a combination of the two.[3] The PDH uses the DS-1 rate (1.544 Mb/s) as its first level, while the SONET uses the OC-1 rate (51.840 Mb/s) as its first level.[4] Networks that use PDH transmission and multiplexing require synchronization of primary multiplexers (channel banks), 64 kb/s circuit switches, and digital cross-connect systems but not transmission and higher level multiplexer systems (Fig. 8a).

[3] SDH is a generic term usually applied to synchronous optical networks outside of North America and is similar to SONET, which is used exclusively in North America.
[4] DS-1 means Digital Signal Level No. 1 and OC-1 means Optical Carrier Level No. 1.

Fig. 8a – Plesiochronous Digital Hierarchy Network Synchronization



Higher order multiplexers (for example, M12 and M13) operate asynchronously. They align DS-1 tributaries into aggregate rates using bit-stuffing mechanisms. These mechanisms allow DS-1 rate tributaries to be used to transport timing between network elements requiring synchronization.

A network based on SONET transmission and multiplexing requires synchronization of not only the network nodes but also the transmission and multiplexing network elements as well (Fig. 8b). DS-1 signals are carried as virtual tributaries in SONET payload at 1.728 Mb/s. SONET uses a pointer adjustment mechanism (byte stuffing) to accommodate expected phase differences between the SONET and the virtual tributaries. The pointer adjustments generate jitter and wander on the DS-1 PDH *tributary* signal output interfaces. Each pointer adjustment causes a phase jump of 8 UI (8 bit periods) at the tributary rate (1.728 Mb/s), or 4.6 µs. Pointer adjustments in a properly timed network are relatively rare. However, the resulting jitter can exceed network limits. This precludes the DS-1 tributaries from being used for timing transport across the SONET (Fig. 8c).

Fig. 8b – SONET Synchronization

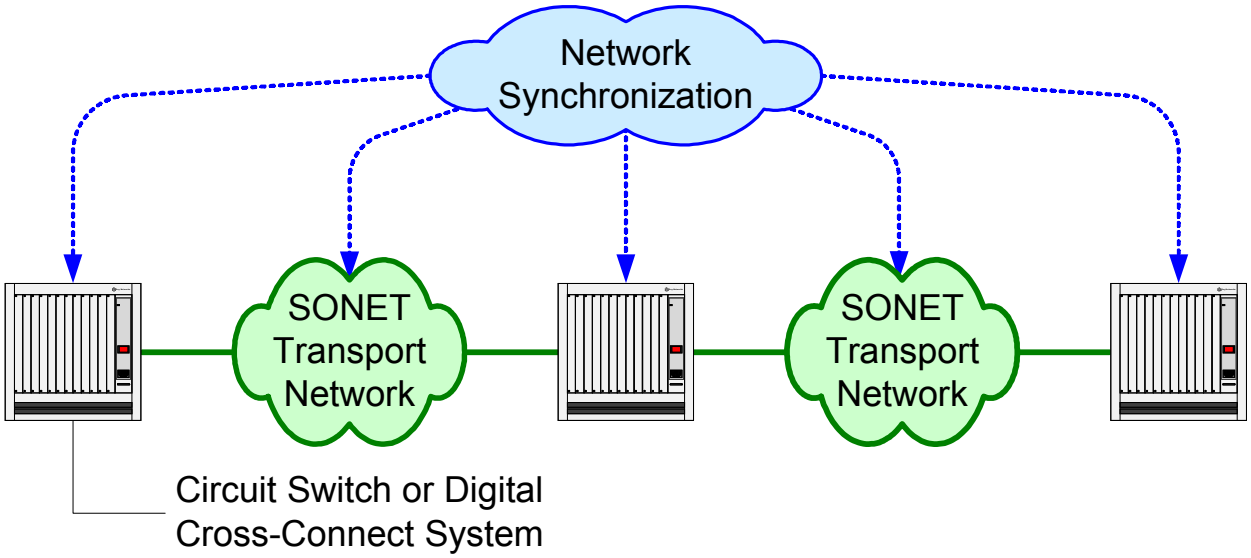
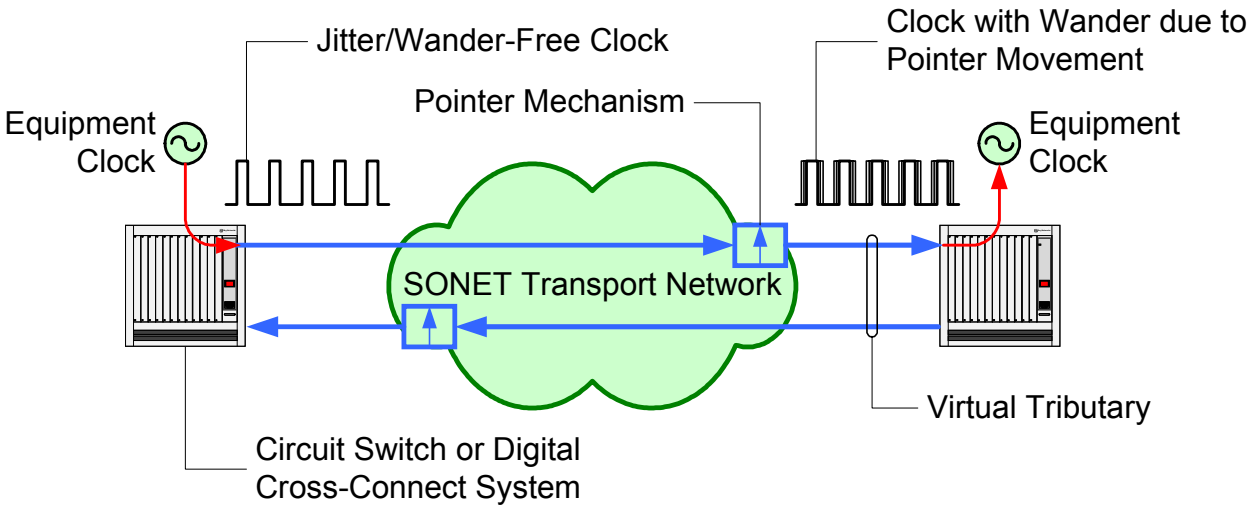
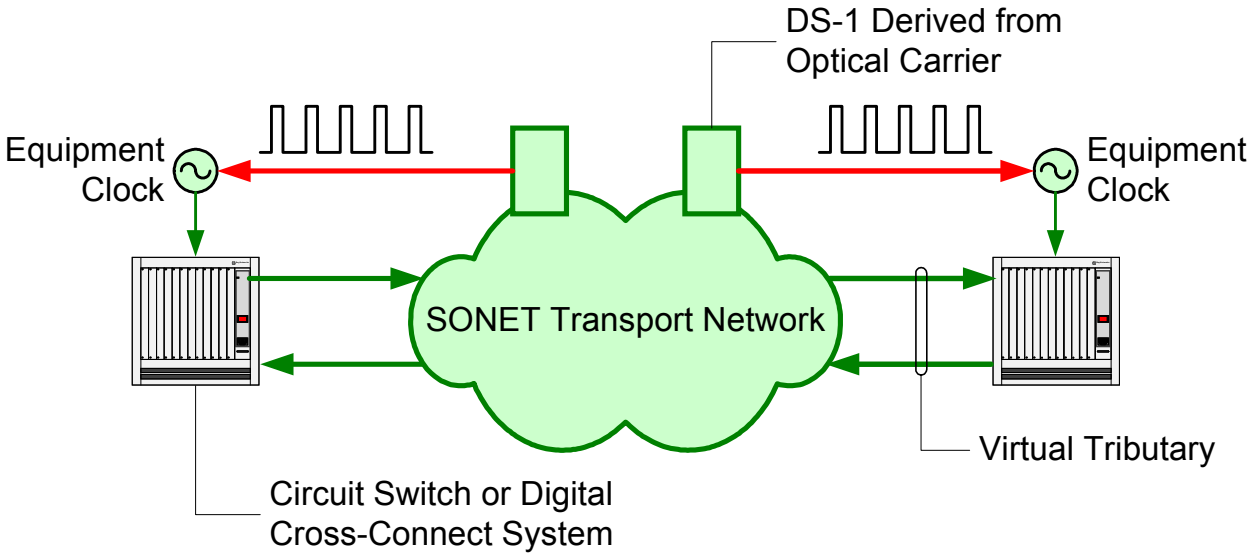


Fig. 8c – Incorrect Use of Tributaries for Timing Transport in the SONET



The best way to provide timing transport through a SONET is to use a DS-1 interface whose timing is derived directly from the optical carrier (Fig. 8d). This is a non-traffic DS-1 interface that is designed specifically for timing transport and is called a *derived DS-1*. However, there are situations where there is no alternative to taking synchronization from a tributary DS-1, such as where a digital switching system does not have an external timing interface and must be timed by an incoming traffic DS-1 or at certain types of wireless Base Transceiver Stations (BTS). These problems can be solved by a retiming unit (RTU, also called a Timing Insertion Unit, or TIU). RTUs are discussed in more detail later.

Fig. 8d – Using DS-1 Signal Derived from the SONET Optical Carrier for Timing Transport



6. ***Switching System Synchronization***

Digital 64 kb/s circuit switches and digital cross-connect systems can only operate in a synchronous manner; that is, all operations must occur at the proper time and in the proper order. Buffers are used to accommodate wander and to minimize frame slips. Buffer size typically is two DS-1 frames, or 386 bits.

Frame Relay and Asynchronous Transfer Mode (ATM) packet switches generally do not require synchronization for switching. However, these types of packet network elements do require synchronization when they terminate services on synchronized digital interfaces. These include ATM Circuit Emulation Service (CES) at the DS-1 rate and IP routers providing Voice-over-IP (VoIP) service that are connected on a digital basis to a 64 kb/s circuit switch.

7. ***Timing Provisioning***

Digital network elements usually have several provisioning options. Fig. 9a through 9e illustrate the range of options that may be available along with a brief description of each. Not all network elements have all options available. Circuit switching systems may be provisioned for either external or line timing, or both. Some current systems presently only allow external timing and some only may be setup for line timing.

Fig. 9a – External Timing
External timing usually provides the highest overall reliability but requires the highest initial investment; however, the initial investment may be less than ongoing operation costs of other methods. Although not obvious from the illustration, the PRS usually is connected to or part of a Synchronization Supply Unit for timing distribution to all network elements in a building.

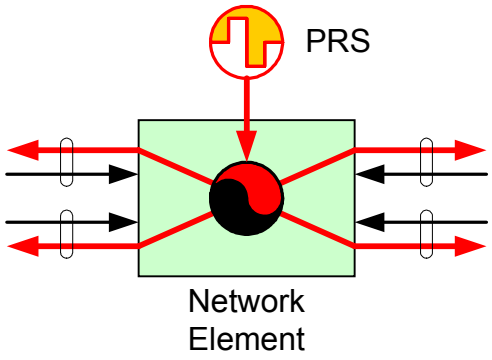


Fig. 9b – Line Timing
When it is not possible to use External Timing because the network element does not have an external timing input or because of cost considerations, line timing is a common provisioning method.

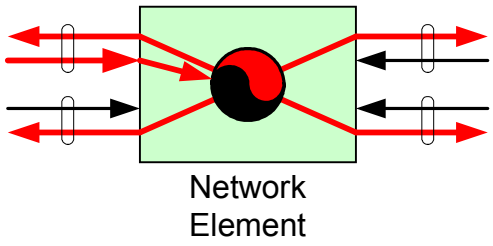


Fig. 9c – Loop Timing
Loop timing typically is used in terminal equipment such as Digital Loop Carrier Remote Terminals and Customer Premises Equipment connected to the public network.

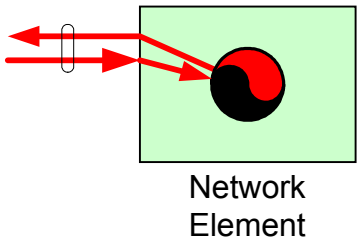


Fig. 9d – Through Timing
Through timing is common in SONET Add-Drop Multiplexers (ADM).

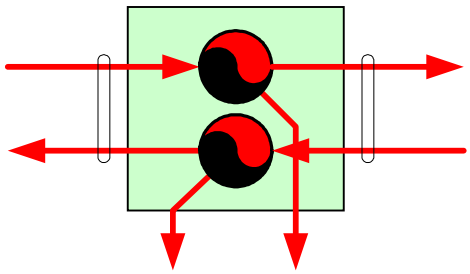
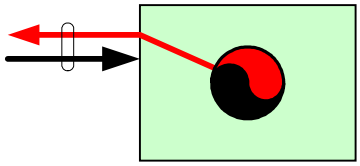


Fig. 9e – Internal Timing
Internal timing can be used successfully in low-speed, point-to-point systems that are not connected to any other networks. The internal clock operates in the free-run mode and is not synchronized to any external reference. This provisioning cannot be used in high-speed networks connected to other networks.



8. Retiming Units (RTU)

Some network elements may not have an external timing input and must be line timed from traffic DS-1 interfaces. These traffic DS-1 interfaces have excessive jitter and wander when carried as virtual tributaries in SONET systems or on satellite circuits, so retiming must be used to improve overall synchronization performance (Fig. 10).

A basic retiming unit has a traffic input, a reference clock input from an SSU, a traffic output and a buffer (Fig. 11). The input traffic signal and reference clock must be traceable to a Stratum 1 timing source. The output traffic signal contains the data from the traffic input and the clock rate from the reference input. Retiming cannot compensate for sustained frequency offset between the traffic and reference inputs because the buffer eventually will overflow or underflow causing slips and data loss. Buffer size normally equals two frames at the DS-1 rate, or 386 bits.

Fig. 10 – Retiming Unit Application

The end office switching system in this example does not have an external timing input, but it can be synchronized to a traffic signal on a DS-1 port. The DS-1 traffic signal from the satellite earth station has excessive jitter and wander, so a Retiming Unit is used to retime the traffic signal and to remove jitter and wander.

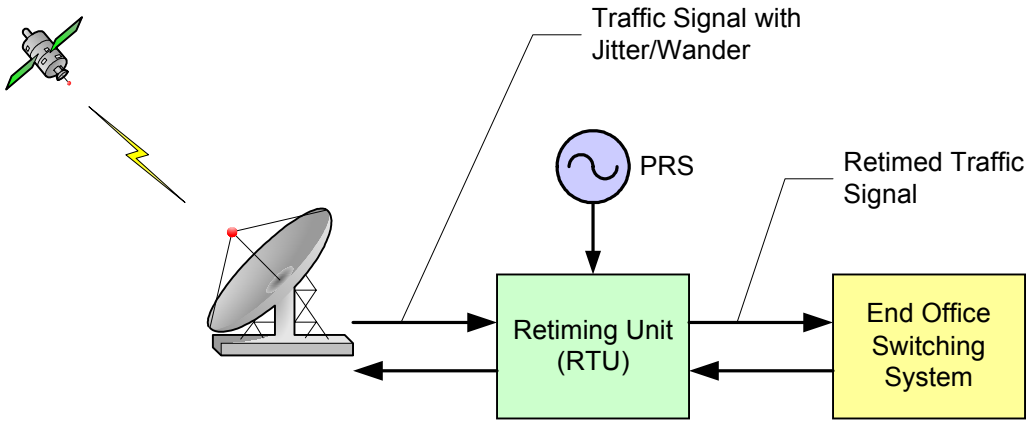
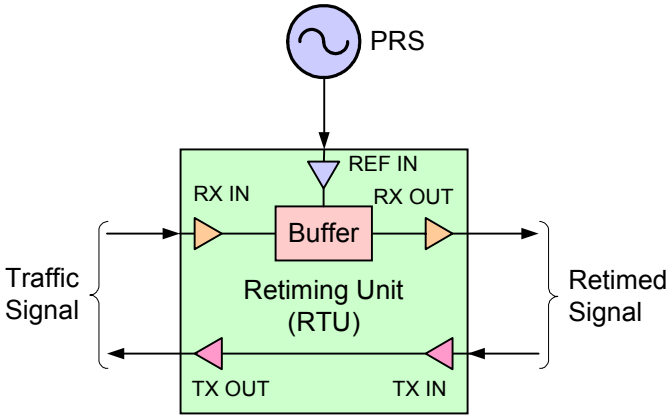


Fig. 11 – Basic Retiming Unit Operation

The data at the RX IN port is written into the buffer at the traffic signal rate. Although the timing for this signal is traceable to a Stratum 1 clock, the signal may have excessive jitter and wander. The data is written out of the buffer to the RX OUT port at the reference clock (PRS) rate. The short-term difference between the traffic and reference clock rates will add or subtract to the buffer fill but, if properly designed, the buffer will never completely fill or completely empty. The TX IN and TX OUT ports are pass-through and are not affected by the retiming operation.



9. References

Standards

ANSI T1.101-1999, Synchronization Interface Standard
ANSI T1.102-1993 (R1999), Digital Hierarchy – Electrical Interfaces
ANSI T1.102.01-1996 (R2001), Digital Hierarchy – VT1.5 Electrical Interface

Industry Practices

GR-378-CORE, Generic Requirements for Timing Signal Generators, Telcordia
GR-436-CORE, Digital Network Synchronization Plan, Telcordia
GR-1244-CORE, Clocks for the Synchronization Network: Common Generic Criteria, Telcordia
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Other

T1X1.3/2000-002R1,Technical Report on Synchronization Network Architecture, T1 Committee (www.t1.org)

10. Revision History

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11. Author Contact Information

Whitham D. Reeve
Reeve Engineers
P.O. Box 190225
Anchorage, AK 99519-0225

Tel +1 907-243-2262
Fax +1 907-243-0234
email: whit@reeve.com
web: www.reeve.com

Appendix I Geostationary Satellites

A geostationary satellite is located above the equator at an orbital radius of approximately 42,164 km (from earth center) and has the same orbital period as the earth, but it does not remain in perfect position. Its orbit can be specified in terms of

- Inclination angle relative the equatorial plane (north-south drift)
- Orbital eccentricity
- East-west drift

The orbital eccentricity can cause a peak-to-peak altitude variation of around 0.2% of the orbit radius, or about 85 km. The east-west and north-south peak-to-peak variation at the end of satellite life is around 0.2° (station keeping of ±0.1°) or about 150 km. These variations are combined as vectors, so the total variation is $(85^2 + 150^2)^{1/2}$ = 172 km, which results in a one-way propagation delay variation of about 0.573 ms or a round-trip delay variation of around 1.15 ms. The satellite moves from its nominal position to the position where maximum delay variation occurs on an 8 hour basis. Therefore, the Doppler shift is 1.15 ms/8 hr = 40 ns/s.

The Doppler shift can be put in terms of data bits at a given rate, which indicates buffer size to accommodate the shift

$$B = D \cdot R$$

where

B = Equivalent number of data bits
D = Doppler shift (seconds)
R = Bit rate (b/s).

In general, two earth station synchronization scenarios exist:

- **Case 1**: Plesiochronous (or pseudo-synchronous) networks at both ends (interfaces at both ends traceable to Stratum 1 clock)
- **Case 2**: Interface at one end traceable to Stratum 1 clock and the other end loop-timed

For **Case 1**, the buffer size is based on data frame size and Doppler shift. At the DS-1 rate (1.544 Mb/s), the equivalent number of bits due to Doppler shift is $1.15 \times 10^{-3} \times 1.544 \times 10^{6}$ = 1,776 bits. Doppler buffers usually are combined with frame buffers in earth station interfaces. The DS-1 data frame is 193 bits. Buffers must be able to accommodate at least two frames and two Doppler shifts (a buffer does not store just one frame or one Doppler shift because it must be able to start at the center and move in both directions). Therefore, the total buffer storage capacity is (2 x 193) + (2 x 1,766) = 3,938 bits. For **Case 2**, the Doppler shift is increased by a factor of 2 to account for the timing passing over the satellite path twice. Therefore, the buffer size for Doppler shift is (4 x 1,766) = 7,064 bits. Note that, in both cases, external equipment (switching system or digital cross-connect system) connected to the earth station interface probably has a frame buffer, which is independent of the buffer in the earth station itself.

In the discussion above, the buffer is based on a single data frame. Higher level multiplex equipment normally buffers a full multi-frame to minimize recovery time after interface failures. The DS-1 SuperFrame consists of 12 data frames (2,316 bits) and the Extended SuperFrame consists of 24 data frames (4,632 bits). Buffers must be at least twice this size, or 4,632 bits (3 ms) for the SF and 9,264 bits (6 ms) for the ESF.